UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Canon U.S.A., Inc., and Canon Inc.,

Petitioners

v.

Slingshot Printing LLC,

Patent Owner

Case No. IPR2022-01414

Patent No. 7,195,341

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,195,341 (CLAIMS 1-5 AND 8)

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 311 and 37 C.F.R. § 42.100 et seq., Petitioners request *Inter Partes* Review ("IPR") of claims 1-5 and 8 (the "Challenged Claims") of U.S. Patent No. 7,195,341 ("the '341 Patent," Ex. 1001), purportedly owned by Slingshot Printing LLC ("Patent Owner").

II. MANDATORY NOTICES

Real Party-in-Interest: The real parties-in-interest are **Canon U.S.A., Inc.** and **Canon Inc.**

Related Matters: The '341 Patent has been asserted against Petitioner Canon U.S.A., Inc. as well as Canon Solutions America, Inc. in *Slingshot Printing LLC v. Canon U.S.A., Inc., et al.*, No. 2:22-cv-00123 (E.D.N.Y.), which was filed on January 7, 2022. The '341 Patent was previously asserted against HP Inc. in *Slingshot Printing LLC v. HP Inc.*, No. 6:19-cv-00549, reassigned as No. 2:20-00187 (W.D. Tex.). That case was dismissed with prejudice on April 1, 2021 following the parties' joint stipulation of dismissal. To the best of Petitioners' knowledge, the '341 Patent has not been asserted against other parties.

Lead Counsel: Dion M. Bregman (Reg. No. 45,645); Back-up Counsel: Amanda S. Williamson (Reg. No. 73,683) and Jason E. Gettleman (Reg. No. 55,202).

Service: Service of any documents may be made on Morgan, Lewis & Bockius LLP, 1400 Page Mill Road, Palo Alto, CA, 94304 (Telephone: 650.843.4000; Fax: 650.843.4001). Petitioners consent to e-mail service at: CanonSlingshotIPRs@morganlewis.com.

III. IDENTIFICATION OF CLAIMS AND GROUNDS

'341 Patent: This patent was filed on September 30, 2004 and has an earliest possible priority date of **September 30, 2004**. It is subject to the pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

Torgerson: U.S. Patent No. 6,412,917 titled "Energy Balanced Printhead Design" to Joseph M. Torgerson, Robert N.K. Browning; Mark H. MacKenzie, and Patrick V. Boyd ("Torgerson," Ex. 1004), was filed January 30, 2001 and published **July 2, 2002**, and is prior art under § 102(b).

Bruce: U.S. Patent No. 7,240,997 titled "Fluid Ejection Device Metal Layer Layouts" to Kevin Bruce, Joseph M. Torgerson, Trudy Benjamin, and Michael D. Miller ("Bruce," Ex. 1005), was filed on **February 25, 2004** and published July 10, 2007, and is prior art under § 102(e).

Furukawa: Japanese Patent Application No. 1996-108536 titled "Recording Head, and Recording Device Using This Recording Head" to Tatsuo Furukawa, Fumio Murooka, Masami Kasamoto, Teruo Ozaki, and Masahiko Tonogaki

("Furukawa," Ex. 1006), was filed on October 13, 1994 and published **April 30, 1996**, and is prior art under § 102(b).

Petitioners request that the Board find each of the Challenged Claims invalid on the following grounds:

Ground	Prior Art	Statutory Basis	Claims
1	Torgerson and Bruce	§ 103	1-5 and 8
2	Furukawa and Torgerson	§ 103	1-5 and 8

IV. CERTIFICATION AND FEES

Petitioners certify that the '341 Patent is available for IPR and that Petitioners are not barred or estopped from requesting this IPR on the grounds identified herein.

Any additional fees may be charged to Deposit Account No. 50,0310 (Order No. 132261-0003).

V. THE BOARD SHOULD NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

To the extent Patent Owner argues that the Board should exercise its discretion by denying institution under § 314(a), such arguments would be unavailing.

As of the filing of this Petition, trial has not been set in the district court litigation asserted by Patent Owner against Defendants for the '341 Patent but would occur no earlier than late 2024 based on the parties' Case Management Schedule

setting *Daubert* motion replies for October 25, 2024 and trial after that date. Ex. 1009 at 6. Thus, the Board's deadline to issue a final written decision will predate the trial date in the concurrent litigation, which counsels in favor of declining to deny institution under 35 U.S.C. § 314(a). *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 at 3 (PTAB Mar. 20, 2020) (precedential). The six non-exclusive factors set forth in *Fintiv* further support declining to deny institution under 35 U.S.C. § 314(a). *Id*. at 5-6.

A. Whether the Court Granted a Stay or Evidence Exists that One May be Granted if a Proceeding is Instituted

Neither party has requested a stay in the District Court, and it is speculative at this point whether a stay would be granted if requested. Staying the corresponding litigation, however, would align with Congressional intent. *See IOENGINE, LLC v. PayPal Holdings, Inc.*, Nos. 18-452-WCB; 18-826-WCB, 2019 WL 3943058, at *3-4 (D. Del. Aug. 21, 2019) ("Congress intended for district courts to be liberal in granting stays."); 157 Cong. Rec. S1363 (daily ed. Mar. 8, 2011) (statement of Sen. Schumer) (Congress intended to place "a very heavy thumb on the scale in favor of a stay being granted"); *NFC Tech. LLC v. HTC Am., Inc.,* 2015 WL 1069111, at *7 (E.D. Tex. Mar. 11, 2015) ("[A]fter the PTAB has instituted review proceedings, the parallel district court litigation ordinarily should be stayed.").

Petitioners submit that the Board should decline to speculate how the District Court might rule on a potential stay request. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) ("In the absence of specific evidence, we will not attempt to predict how the district court in the related district court litigation will proceed because the court may determine whether or not to stay any individual case, including the related one, based on a variety of circumstances and facts beyond our control and to which the Board is not privy.").

As such, this factor is neutral.

B. Proximity of the Court's Trial Date to the Board's Projected Statutory Deadline for a Final Written Decision

The district court case involving the '341 Patent is in its early stage with no trial date yet set. The parties had an Initial Conference with the court on July 5, 2022 during which the court entered the parties' Case Management Schedule. The last set date in the schedule is Reply *Daubert* motions set for October 25, 2024, which means trial cannot occur until after October 25, 2024. Ex. 1009 at 6. Moreover, the median time to trial in the Eastern District of New York is 48.9 months (~4 years).

As the final written decision must be issued within one year of institution, absent extension of up to six months for good cause, the final written decision will be issued well before any trial date that may occur under the parties' current Case

Management Schedule or under the median time to trial in the Eastern District of New York.

As such, this factor weighs against discretionary denial.

C. Investment in the Parallel Proceeding by the Court and the Parties

Fact discovery is in the very early stages and expert discovery has not yet begun. Claim construction proceedings are not set to start until April 7, 2023 when the parties exchange a list of disputed terms for construction. Ex. 1009 at 4.

Under the parties' schedule, by the time of the institution deadline, the Court would not have issued any claim construction rulings and likely would neither have ruled on any dispositive motions nor considered any invalidity issues based on the prior art. Thus, institution would save substantial resources of the parties and the District Court, which could rely upon any PTAB claim constructions while also considering whether a stay is warranted to avoid duplicating efforts.

As such, this factor weighs against discretionary denial.

D. Overlap Between Issues Raised in the Petition and in the Parallel Proceeding

Defendants have not yet served their invalidity contentions in the district court litigation because those are not due until October 17, 2022. Ex. 1009 at 4. The invalidity contentions will include the prior art cited in this Petition. As the Board has noted, when overlap exists between the invalidity issues in the Petition and the

district court this "overlap may inure to the district court's benefit, however, by simplifying issues for trial should we reach our determination on the challenges raised in the Petition before trial." *MED-EL v. Sonova AG*, IPR2020-00176, Paper 13 at 15 (PTAB June 3, 2020) (declining to exercise discretion under § 314(a)). Given that the final written decision will issue before the trial date, it is more efficient for the Board to handle any overlapping prior art.

As such, this factor weighs against discretionary denial.

E. Whether the Petitioners and the Defendants in the Parallel Proceeding are the Same Party

Petitioner Canon U.S.A., Inc. is a defendant in the parallel district court proceeding. Petitioner Canon Inc. is not a party to the parallel litigation. Although this factor arguably weighs in favor of discretionary denial, this interpretation of the factor has been questioned by the Board. *See Cisco v. Ramot*, IPR2020-00122, Paper 15 at 10 (dissent).[1]

F. Other Circumstances that Impact the Board's Exercise of Discretion, Including the Merits

This factor favors institution and is dispositive under the Guidance issued by the USPTO on June 21, 2022 because the unpatentability challenges here are

[1] Note that Canon Solutions America, Inc. in the parallel district court litigation is not a real-party-in interest in this proceeding.

compelling and rely on references that were not before the Office. Additionally, this IPR is the only challenge to the '341 Patent that has been before the Board, which favors institution. There is also a strong public interest against "leaving bad patents enforceable," which also favors institution. *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). Finally, given the Board's technically trained judges are well-suited to assess the patentability grounds presented here, it is more efficient for the Board to address the patentability of the '341 Patent.

As such, this factor weighs against discretionary denial.

For the foregoing reasons, instituting IPR would be an efficient use of Board resources and provide the most efficient use of judicial resources for overall system efficiency, fairness, and patent quality.

VI. BACKGROUND

A. The '341 Patent

The '341 Patent describes "[a] semiconductor substrate for a micro-fluid ejection device," and explains that "**[m]icro-fluid ejection devices** continue to be used in a wide variety of applications, **including ink jet printers**." Ex. 1001 at Abstract, 1:12-13.[2] The '341 Patent describes the competing need of increased

[2] Emphasis added unless otherwise indicated.

functionality on a semiconductor substrate with the need to reduce the size of the substrate noting:

> As the complexity of micro-fluid ejection devices increases, there is a need to include more functions on semiconductor substrates for the devices. However, there is a competing need to maintain or reduce the size of the substrates so as to minimize the cost of the ejection devices.

Ex. 1001 at 1:22-26.

The '341 Patent describes the purported inventive layout for the semiconductor substrate noting:

> A plurality of **micro-fluid ejection actuators are in a columnar array** on a device surface of a semiconductor substrate **adjacent the fluid supply slot**. A plurality of **power transistors are formed in a columnar array adjacent the ejection actuators**. The power transistors occupy a power transistor area of the substrate and are **interconnected to the ejection actuators in a first metal conductor layer**. A **columnar array of logic circuits are formed adjacent the power transistors**. The logic circuits occupy a logic circuit area of the substrate and are **interconnected to the power transistors in a polysilicon conductor layer**. A **second metal layer** is deposited on the semiconductor substrate to **provide a power buss and a ground buss** to the ejection actuators. The **power buss overlaps at least a portion of the power transistor active area** and the **ground buss overlaps at least a portion of the logic circuit area**.

Ex. 1001 at 1:65-2:14.

Figure 1 depicts a plan view of "semiconductor substrates for micro-fluid ejection heads" according to the invention. Ex. 1001 at 2:38-40. As seen in Figure 1, the substrate (10) includes three fluid supply slots (14, 16, 18; brown); a plurality of fluid ejection actuators (26) disposed in columnar arrays (30, 32, 34; red) and adjacent the fluid supply slots (14, 16, 18; brown); power transistors (44) included in columnar arrays (48, 50, 52; green) adjacent the columnar arrays (30, 32, 34; red) of fluid ejection actuators (26); and control logic arrays (58, 60, 62; yellow) disposed adjacent the columnar arrays (30, 32, 34; red) of power transistors (44). Ex. 1001 at Fig. 1, 2:59-3:36.

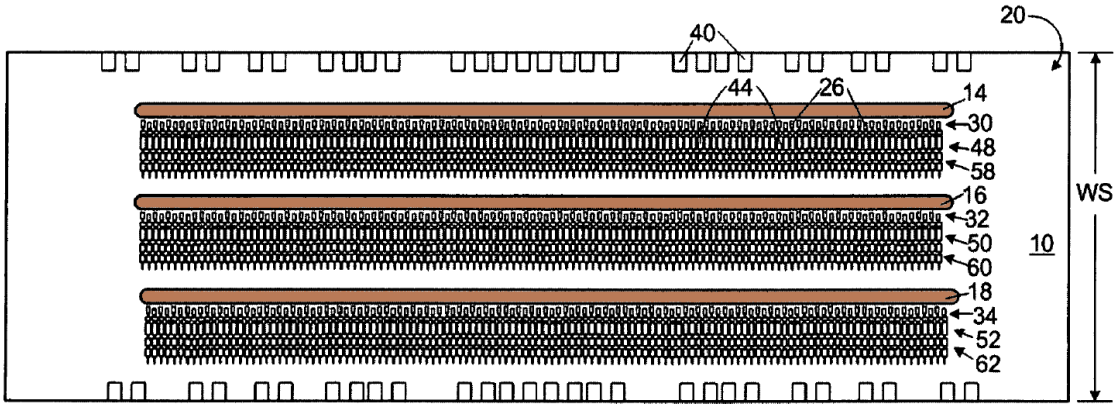
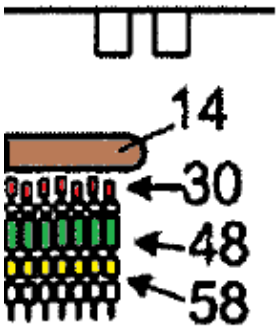


FIG. 1



Ex. 1001 at Fig. 1[3].

As seen in Figure 8, "a power buss 130 [purple] is routed over at least a portion of an active area 132 [green] for the power transistor array 48, 50, or 52," and "the ground buss 136 [blue] is disposed adjacent the power buss 130 [purple] in the second metal conductive layer 74" and "overlies at least a portion of the control logic area 128 [yellow]." Ex. 1001 at Fig. 8, 5:48-50, 58-61.

[3] Annotations and coloring added to figures unless otherwise indicated.

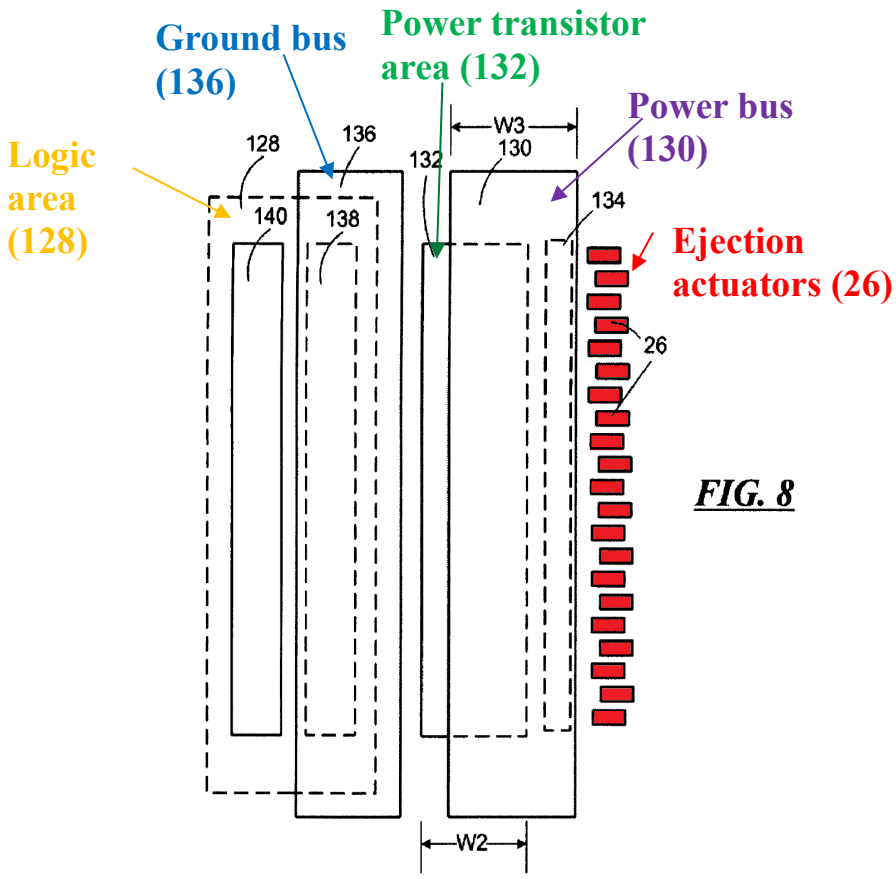


FIG. 8

During prosecution of the application leading to the '341 Patent, the Examiner issued his Notice of Allowance following the Applicant's response to a Restriction Requirement and made no prior art rejections. Ex. 1003 at 46, 52, 58-65; *see also* Ex. 1007 ¶¶ 30-31. In the Notice of Allowance, the Examiner noted the "prior art does not disclose, suggest, or render obvious" and then listed all elements of claim 1. Ex. 1003 at 62-63; Ex. 1007 ¶ 31. The Examiner was not aware during prosecution of any of the references cited herein.

B. The Prior Art

None of the references cited in this Petition were considered by the Patent Office during the prosecution of the application leading to the '341 Patent. Indeed, the Patent Office issued a Notice of Allowance without issuing any office action rejecting the claims based on the prior art. Ex. 1003 at 58-65.

1. Torgerson

During prosecution, the Examiner was not aware of Torgerson (Ex. 1004). Torgerson describes a substrate for an ink jet printhead that has a nearly identical layout to the '341 Patent.

Just like the '341 Patent, Torgerson describes a substrate (die 11 comprising a substrate such as silicon) including **three ink feed slots (71, brown in Fig. 1A below)**; a columnar array (61, red) of ink drop generators comprising **micro-fluid ejection actuators (heater resistors 56, red in Fig. 1A below)** disposed adjacent each of the ink feed slots (71, brown); and a **power conductor (traces 86a, 86b, 86c, 86d; purple in Fig. 1A below)**. Ex. 1004 at Fig. 1A, 2:57-65, 3:66-4:5, 4:36-48, 5:59-6:4; Ex. 1007 ¶¶ 62-76, 97-105.

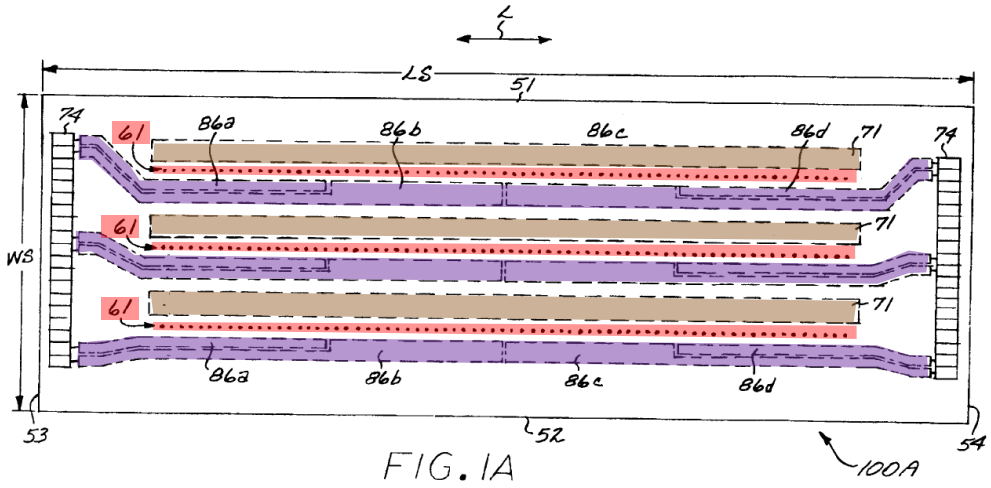
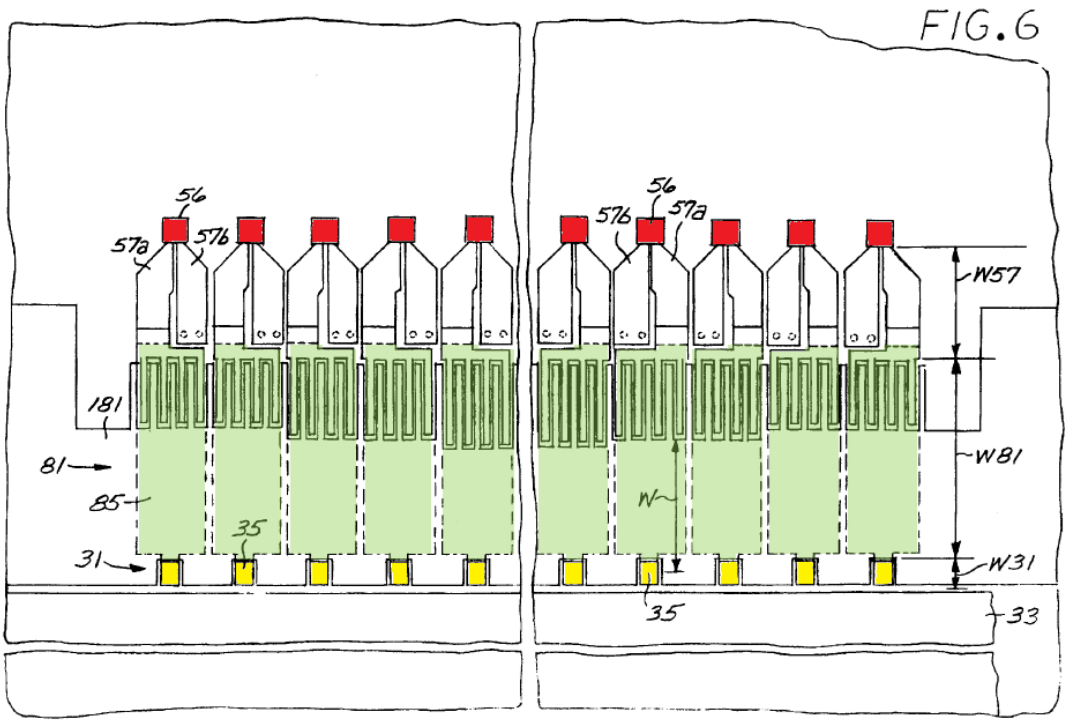


FIG. 1A

Ex. 1004 at Fig. 1A.

Just like the '341 Patent, Torgerson discloses a plurality of **power transistors (FET drive circuits 85, green in Fig. 6 below)** disposed in a columnar array (81) adjacent the **heater resistors (56, red in Fig. 6 below)** and **logic circuits (decoder logic circuits 35, yellow in Fig. 6 below)** disposed in a columnar array adjacent the **FET drive circuits (85, green in Fig. 6 below)**. Ex. 1004 at Fig. 6, 4:65-5:6, 5:24-41; Ex. 1007 ¶¶ 77-96.



Ex. 1004 at Fig. 6.

Just like the '341 Patent, Torgerson describes the FET drive circuits 85 as being connected to the heater resistors 56 noting the "heater resistor leads 57a are **formed in the [first] metallization layer 111d (FIG. 5) of the thin film substructure 11**, as are the heater resistor leads 57b, and the drain and source electrodes of the FET drive circuits 85." Ex. 1004 at 5:19-23; *see also id.* Fig. 7, 3:2-4; Ex. 1007 ¶¶ 77-84. Just like the '341 Patent, Torgerson also describes the decoder logic circuits 35 as being connected through a **polysilicon conductor layer** to the FET drive circuits 85. Ex. 1004 at Fig. 9, 2:42-44, 7:32-44, 8:48-53; Ex. 1007 ¶¶ 85-96.

Just like the '341 Patent, Torgerson describes the **power conductor (traces 86a-86d)** disposed in overlapping relationship with at least a portion of the power transistor active area. Ex. 1004 at Fig. 8, 5:59-6:4; Ex. 1007 ¶¶ 97-105.

2. Bruce

The Examiner was not aware of Bruce (Ex. 1005) during prosecution. Bruce teaches a layout for a "fluid ejection device" that "comprises a first metal layer and a second metallayer [*sic*]." Ex. 1005 at Abstract.

Just like the '341 Patent, Bruce teaches "[r]outing the second-metal-layer **ground portion 8 [blue] through the area of the second metal layer 11** that **overlies logic portions 5 [yellow]**." Ex. 1005 at Fig. 1, 2:50-63; Ex. 1007 ¶¶ 110-112.

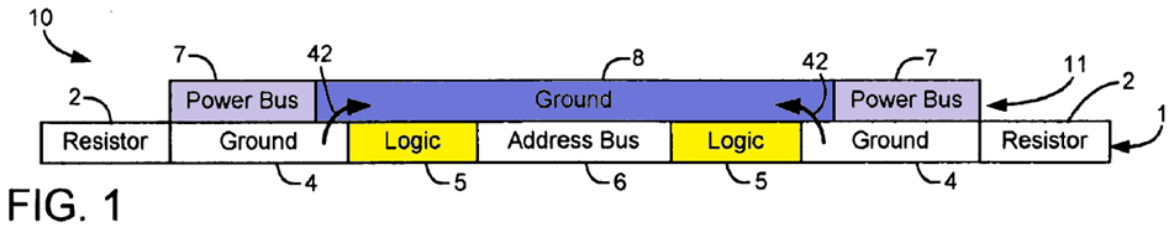


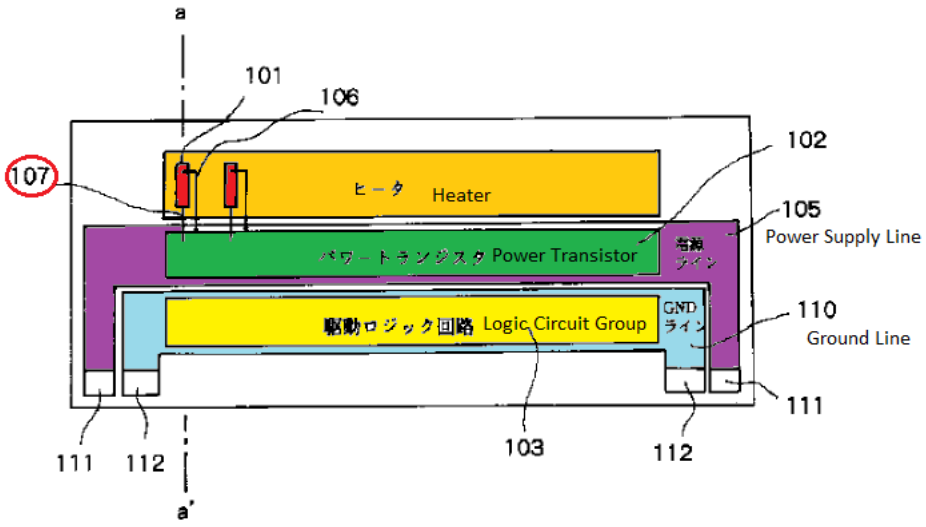
FIG. 1

Ex. 1005 at Fig. 1.

3. Furukawa

The Examiner was not aware of Furukawa (Ex. 1006) during prosecution. Furukawa states the "present invention . . . purposes to provide a **more miniaturized recording head using a compact board,** and a recording device having this recording head." Ex. 1006 at [0012].

Just like the '341 Patent, Furukawa teaches the layout mounted on a substrate noting that "**101 [red in Fig. 3 below] is a heater, 102 [green in Fig. 3 below] is a power transistor, and 103 [yellow in Fig. 3 below] is a drive logic circuit group** comprising a shift register, a latch circuit, a switch, etc." Ex. 1006 at [0023]. "[T]he **power supply line 105 [purple in Fig. 3 below]** is formed of Al (aluminum or alloy containing aluminum) wiring in the second layer, and is positioned on the power transistor 102 element," and "**a GND line 110 [blue in Fig. 3 below]** is formed of Al wiring in the second layer" and is positioned in overlapping relationship with drive logic circuit elements 103. Ex. 1006 at [0023, 0026], Figs. 3-4.



Ex. 1006 at Fig. 3.

VII. LEVEL OF SKILL

A person having ordinary skill in the art ("PHOSITA") at the time of the alleged invention would have been a person holding at least a Bachelor's or Master's

level college degree in Mechanical Engineering, Materials Science, Physics, Electrical Engineering, or a related field, and at least two years of training or experience in the design of inkjet printheads or semiconductor circuit layout. Ex. 1007 ¶ 58.

VIII. CLAIM CONSTRUCTION

Claims are given the same construction as they are given in district court pursuant to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Petitioners propose that the claim terms in the Challenged Claims should be afforded their plain and ordinary meaning.

IX. ARGUMENT

A. Ground #1: Claims 1-5 and 8 are rendered obvious by Torgerson and Bruce

1. Claim 1[4]

Preamble 1[P] "A semiconductor substrate for a micro-fluid ejection device, the substrate comprising":

The recitation in the preamble requiring "for a micro-fluid ejection device" is not limiting because it merely recites the intended use of the purported invention. *See, e.g., Kaidi LLC et al. v. Limoss US, LLC*, IPR2019-01184, Paper 16 at 12-13 (PTAB Dec. 11, 2019). The body of claim 1 fully and intrinsically sets forth all the

[4] A full claim listing can be found in the Appendix.

limitations with no reference being made to a "micro-fluid ejection device" anywhere in the claim's body. Thus, no life and meaning for the claim is provided in the preamble, and it is non-limiting. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999); *see also Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997) ("where a patentee defines a **structurally complete invention** in the claim body and uses the preamble only to **state a purpose or intended use** for the invention, the preamble is **not a claim limitation**.").

Even if limiting, Torgerson discloses "**[a] semiconductor substrate for a micro-fluid ejection device**." Ex. 1007 ¶¶ 62-68.

In particular, the **die 11 comprising a substrate such as silicon** of Torgerson corresponds to the claimed semiconductor substrate, which is included in the **printhead 100A** that corresponds to the claimed micro-fluid ejection device. Ex. 1007 ¶¶ 62-68.

Torgerson explains in his Background section that:

> A typical Hewlett-Packard **ink jet printhead includes** an array of precisely formed nozzles in an orifice plate that is attached to an ink barrier layer which in turn is attached to **a thin film substructure that implements ink firing heater resistors and apparatus for enabling the resistors.** The ink barrier layer defines ink channels including ink chambers disposed over associated ink firing resistors, and the nozzles in the orifice plate are aligned with associated ink chambers. . . . The

> **thin film substructure is typically comprised of a substrate such as silicon** on which are formed various thin film layers that form ink film ink firing resistors, apparatus for enabling the resistors, and also interconnections to bonding pads that are provided for external electrical connections to the printhead.

Ex. 1004 at 1:29-45.

Torgerson further explains that Figures 1-4A and 1B-4B depict "unscaled schematic plan views and perspective views of **ink jet printheads 100A**, 100B in which the invention can be employed and which generally includes (a) **a thin film substructure or die 11 comprising a substrate such as silicon** and having various thin film layers formed thereon, (b) an ink barrier layer 12 disposed on the thin film substructure 11, and (c) an orifice or nozzle plate 13 laminarly attached to the top of the ink barrier 12." Ex. 1004 at 2:57-65. Thus, **die 11 comprising a substrate such as silicon corresponds to the claimed semiconductor substrate**. Ex. 1007 ¶ 64.

The ink jet printhead of Figure 1A is illustrated in Figure 3A, which Torgerson notes depicts "a schematic, partially broken away perspective view of the ink jet printhead of FIG. 1A," with "die 11 [yellow] comprising a substrate such as silicon." Ex. 1004 at 2:22-23, 61-62.

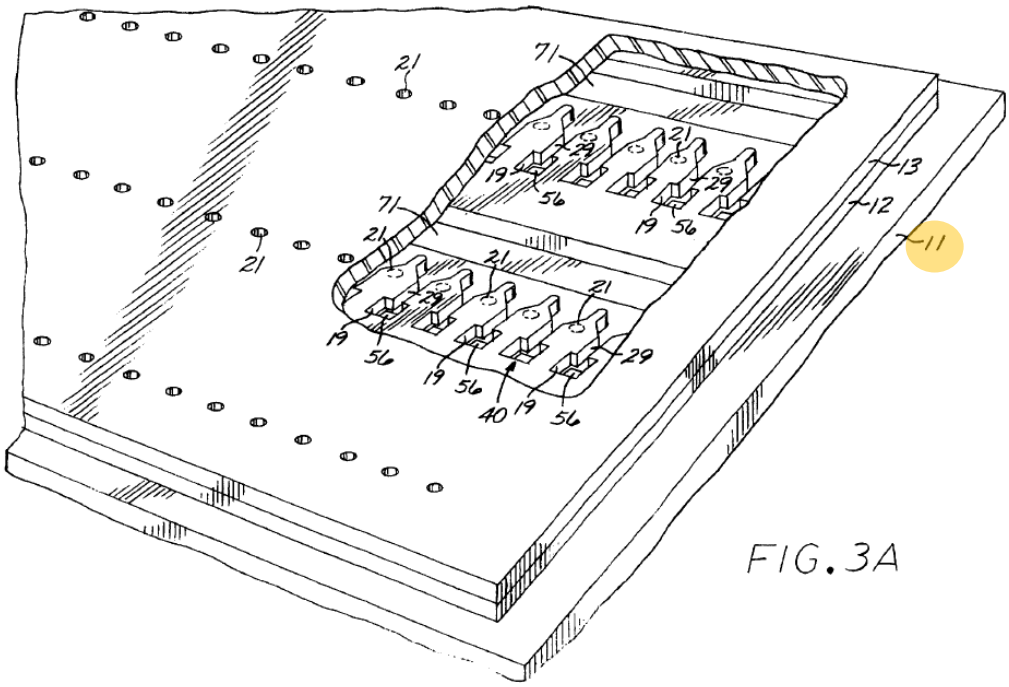


FIG. 3A

Ex. 1004 at Fig. 3A.

The die 11 comprising a substrate such as silicon is thus formed on the **ink jet printhead 100A**, which corresponds to the claimed "micro-fluid ejection device." Ex. 1007 ¶ 66.

A PHOSITA would have understood the term "micro-fluid ejection device" is synonymous with Torgerson's ink jet printhead. Ex. 1007 ¶ 66. Torgerson explains that "an ink jet image is formed pursuant to precise placement on a print medium of ink drops emitted by an **ink drop generating device known as an ink jet printhead**." Ex. 1004 at 1:18-20. Moreover, the '341 Patent states "**[m]icro-fluid ejection devices** continue to be used in a wide variety of applications, including **ink jet printers**." Ex. 1001 at 1:12-13

Therefore, Torgerson discloses "**[a] semiconductor substrate** [e.g., die 11 comprising a substrate such as silicon] for a **micro-fluid ejection device** [e.g., printhead 100A]." Ex. 1007 ¶¶ 62-68.

Limitation 1[A] "a plurality of micro-fluid ejection actuators disposed in a columnar array adjacent a fluid supply slot in the semiconductor substrate":

Torgerson discloses this limitation. Ex. 1007 ¶¶ 69-76.

A PHOSITA would have understood that the term "micro-fluid ejection actuator[ ]" refers to the part of the printhead that causes ink to be ejected from the nozzle, and heater resistors represent one type of a micro-fluid ejection actuator. Ex. 1007 ¶ 70. Indeed, the '341 Patent states "[e]jection actuator 26 is **preferably a heater resistor**." Ex. 1001 at 3:54-55.

Like the '341 Patent, Torgerson utilizes a plurality of **heater resistors 56** that correspond to the claimed plurality of micro-fluid ejection actuators and are disposed in the semiconductor substrate. Ex. 1007 ¶ 71. Torgerson explains, "[t]he thin film **substructure 11 [which corresponds to the claimed semiconductor substrate]** comprises an integrated circuit die that is formed for example pursuant to conventional integrated circuit techniques, and as schematically depicted in FIG. 5 **generally includes . . .a resistor layer 111c, and a first metallization layer 111d**." Ex. 1004 at 2:66-3:4. Torgerson continues noting "**[t]hin film heater resistors 56** are formed by the respective patterning of the **resistor layer 111c and the first**

metallization layer 111d." Ex. 1004 at 3:9-11. Thus, the heater resistors 56 are disposed in the semiconductor substrate of Torgerson. Ex. 1007 ¶ 71.

Like the '341 Patent, Torgerson utilizes **ink feed slots 71** that correspond to the claimed fluid supply slot. Torgerson explains that "**[t]he thin film substructure 11** of the printhead 100A of FIGS. 1A, 2A, 3A, 4A more particularly includes **three ink feed slots 71** that are aligned with the reference axis L, and are spaced apart from each other transversely relative to a reference axis L." Ex. 1004 at 4:36-40; *see also* Ex. 1004 at 3:66-4:5.

As seen in Figure 4A, which depicts "an unscaled schematic partial top plan illustration of the ink jet printhead of FIG. 1A," **heater resistors 56 (red)** are disposed in a columnar array (61) adjacent each of the **ink feed slots 71 (brown)**. Ex. 1004 at Fig. 4A, 2:26-27, 3:66-4:5, 4:36-48.

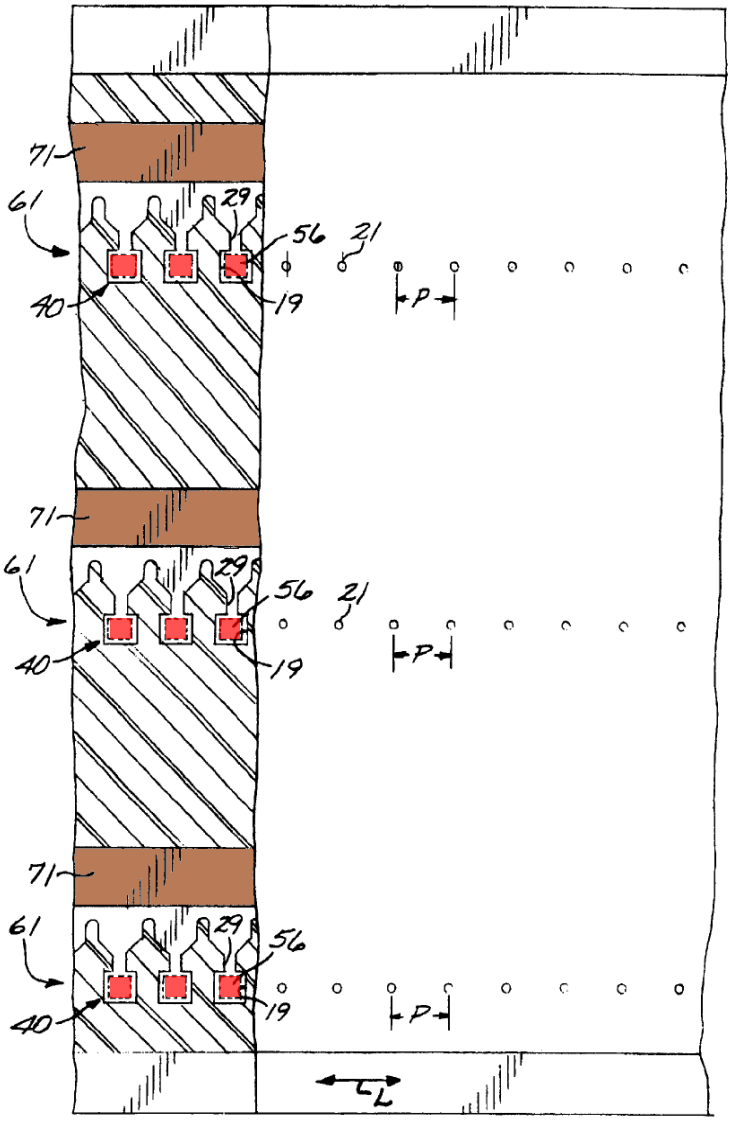


FIG. 4A

Ex. 1004 at Fig. 4A.

Torgerson explains that "[i]nsofar as each of the ink drop generators 40 **includes a heater resistor 56, the heater resistors are accordingly arranged in columnar groups or arrays** that correspond to the columnar arrays of ink drop

generators," and "the heater resistor arrays or groups will be referred to by **the same reference number 61**." Ex. 1004 at 4:29-34

Torgerson also notes:

> The ink drop generators 40 are arranged in **columnar arrays or groups 61** that extend along a reference axis L and are spaced apart from each other laterally or transversely relative to the reference axis L. The **heaters resistors 56 of each ink drop generator group** are generally aligned with the reference axis L and have a predetermined center to center spacing or nozzle pitch P along the reference axis L.

Ex. 1004 at 3:66-4:5.

Therefore, Torgerson discloses "a **plurality of micro-fluid ejection actuators** [e.g., heater resistors 56] disposed in a **columnar array** [e.g., columnar array 61 shown in Fig. 4A] adjacent a **fluid supply slot** [e.g., ink feed slots 71] in the **semiconductor substrate** [e.g., die 11 comprising a substrate such as silicon]." Ex. 1007 ¶¶ 69-76.

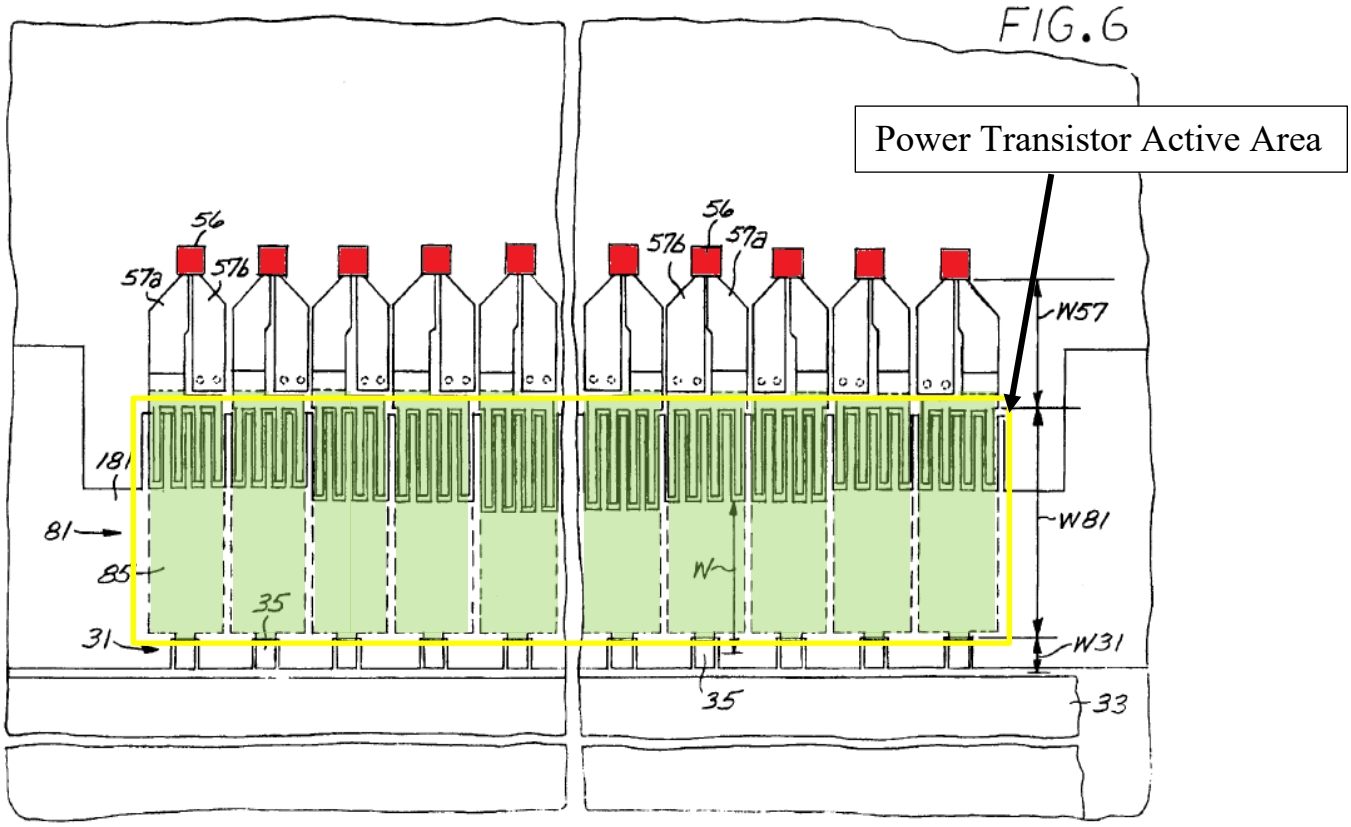
Limitation 1[B] "a plurality of power transistors disposed in a columnar array adjacent the ejection actuators and connected through a first metal conductor layer to the ejection actuators, the columnar array of power transistors occupying a power transistor active area of the substrate":

Torgerson discloses this limitation. Ex. 1007 ¶¶ 77-84.

In Torgerson, **the FET drive circuits 85 correspond to the claimed plurality of power transistors**. Ex. 1007 ¶ 78. "FET" refers to a field effect transistor, which can control the flow of current in a semiconductor substrate. *Id*. As Torgerson explains, "ink firing energy PS is provided to the heater resistor 56 if the associated FET drive circuit is ON." Ex. 1004 at 5:38-40.

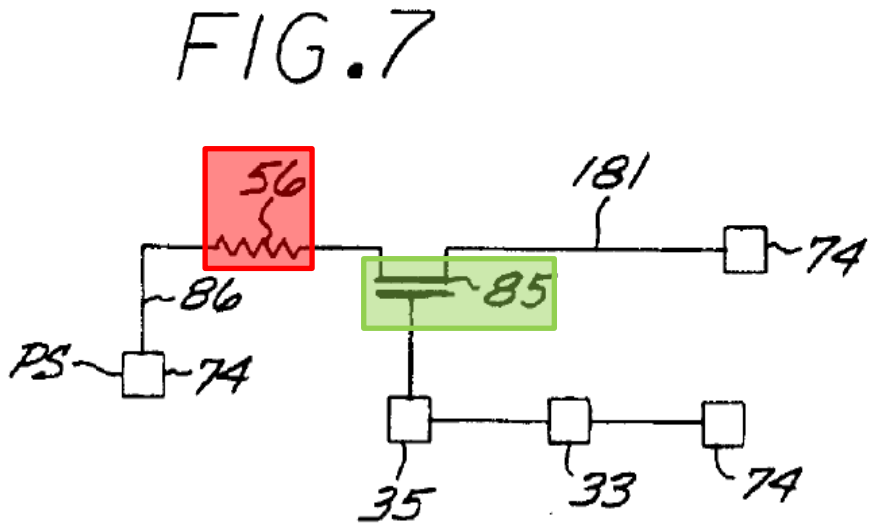
Torgerson explains that "**columnar FET drive circuit arrays 81** [are] formed in the thin film substructure 11 of the printheads 10A [*sic*] . . . as schematically depicted in FIG. 6" and "[e]ach **FET drive circuit array 81 includes** a **plurality of FET drive circuits 85** having drain electrodes **respectively connected to respective heater resistors 56** by heater resistor leads 57a." Ex. 1004 at 4:65-5:6.

As seen in Figure 6, the **plurality of FET drive circuits 85 (green)** are disposed in a columnar array adjacent the columnar array of **heater resistors 56 (red)**. Ex. 1004 at Fig. 6, 4:65-5:6. As in the '341 Patent, the area occupied by the columnar array of power transistors (as depicted by the yellow box) forms the **power transistor active area** of the substructure 11. Ex. 1007 ¶ 80; *see also* Ex. 1001 at 1:48-49 ("The columnar array of power transistors occupies a **power transistor active area** of the substrate.").



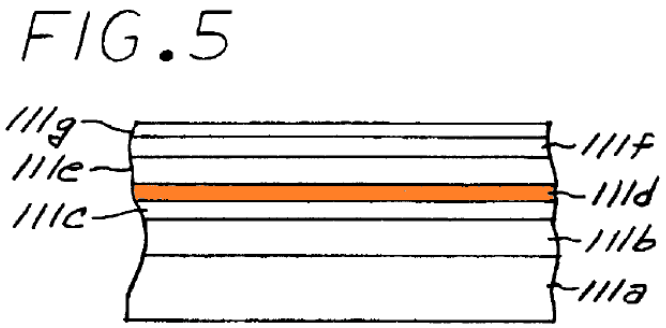
Ex. 1004 at Fig. 6.

Figure 7 depicts the connection between each heater resistor 56 (red) and its associated FET drive circuit 85 (green) noting that "each **heater resistor 56 [red] is connected to the drain terminal of an associated FET drive circuit 85 [green]**." Ex. 1004 at 5:37-42.



Ex. 1004 at Fig. 7.

This connection between the plurality of FET drive circuits 85 and the heater resistors 56 is provided in a first metal conductor layer. Ex. 1007 ¶¶ 82-83. Torgerson explains that the "FET drive circuits 85 hav[e] drain electrodes respectively connected to respective heater resistors 56 by **heater resistor leads 57a**." Ex. 1004 at 5:3-6. The "heater resistor leads 57a are **formed in the metallization layer 111d (FIG. 5) [orange] of the thin film substructure 11**, as are the heater resistor leads 57b, and the drain and source electrodes of the FET drive circuits 85." Ex. 1004 at 5:19-23. Torgerson describes metallization layer 111d as the "**first metallization layer**." Ex. 1004 at 3:2-4.



Ex. 1004 at Fig. 5.

Although Torgerson does not expressly call the "first metallization layer 111d" a first metal "conductor" layer as recited in the '341 Patent, a PHOSITA would have understood that as layer 111d is metal, it is a conductor. Ex. 1007 ¶ 83.

Therefore, Torgerson discloses "a **plurality of power transistors** [e.g., FET drive circuits 85] disposed in a **columnar array** [e.g., columnar array 81 as shown in Fig. 6] adjacent the **ejection actuators** [e.g., heater resistors 56] and connected through a **first metal conductor layer** [e.g., first metallization layer 111d] to the **ejection actuators** [e.g., heater resistors 56], the columnar array of power transistors occupying a **power transistor active area** [e.g., yellow box in annotated Figure 6 above] of the **substrate** [e.g., die 11 comprising a substrate such as silicon]." Ex. 1007 ¶¶ 77-84.

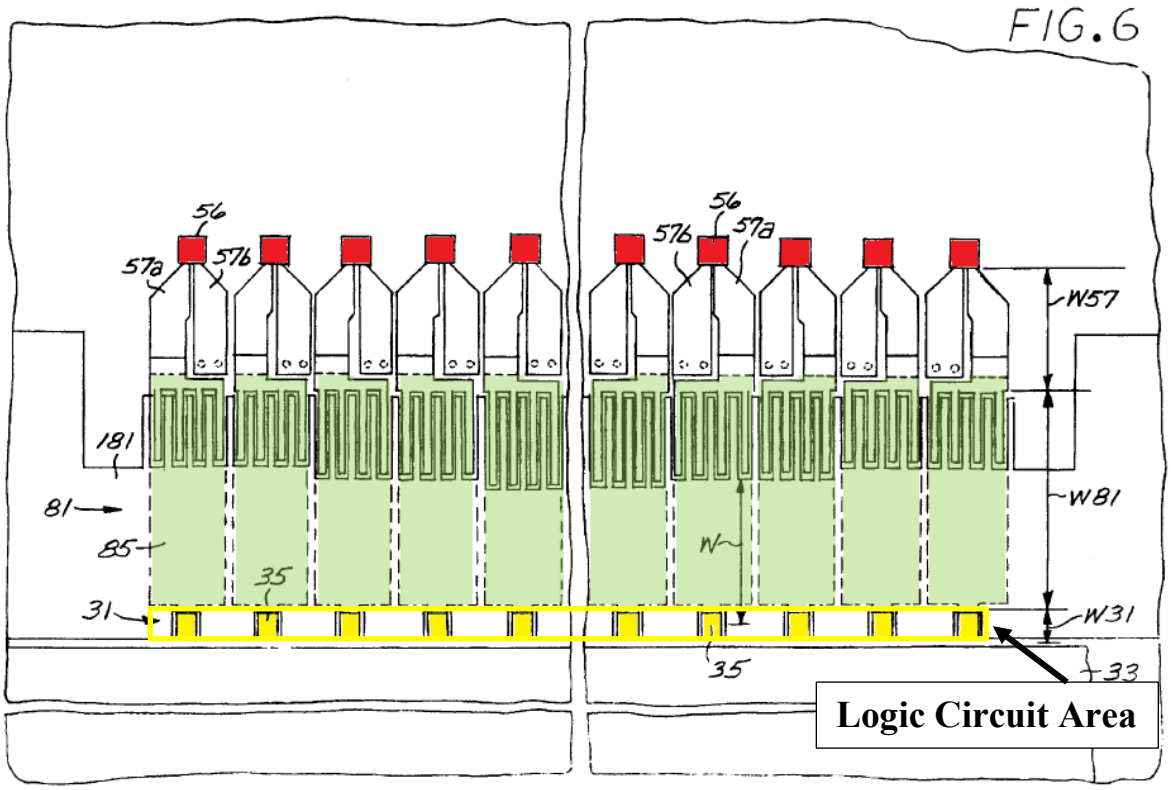
Limitation 1[C] "a columnar array of logic circuits disposed adjacent the columnar array of power transistors and connected through a polysilicon

conductor layer to the power transistors, the columnar array of logic circuits occupying a logic circuit area of the substrate":

Torgerson discloses this limitation. Ex. 1007 ¶¶ 85-96.

In Torgerson, the **decoder logic circuits 35** correspond to the claimed logic circuits, which are disposed in a columnar array. Ex. 1007 ¶¶ 85-96. As Torgerson explains "[t]he FET drive circuits 85 of each columnar array of FET drive circuits **are controlled by an associated columnar array 31 of decoder logic circuits 35**." Ex. 1005 at 5:24-26.

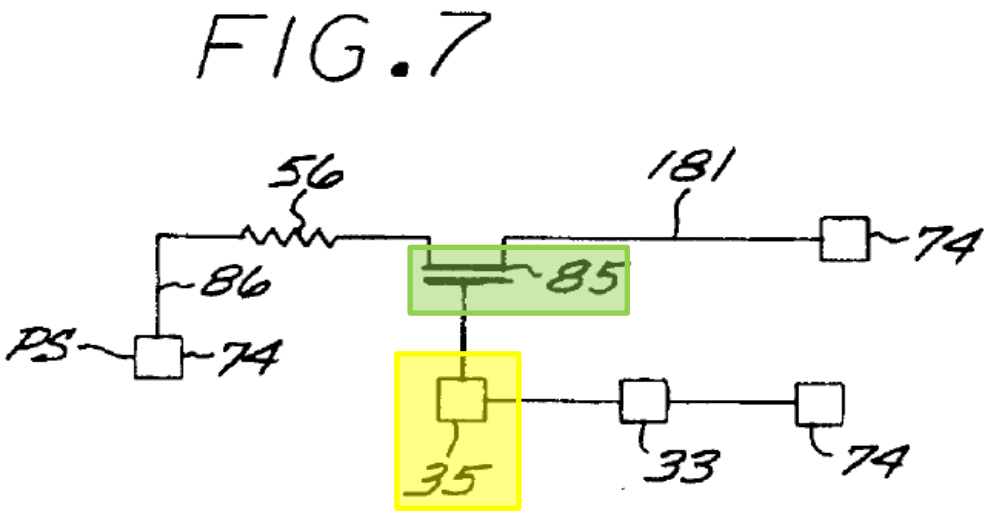
Figure 6 of Torgerson illustrates this with the **decoder logic circuits 35 (yellow) being disposed in a columnar array 31** adjacent the columnar array of FET drive circuits 85 (green). As in the '341 Patent, the area occupied by the columnar array of logic circuits (as depicted by the yellow box) forms the **logic circuit area** of the substructure 11. Ex. 1007 ¶ 87; *see also* Ex. 1001 at 1:53-54 ("The columnar array of logic circuits occupies a **logic circuit area** of the substrate.").



Ex. 1004 at Fig. 6.

Torgerson also teaches that the columnar array of logic circuits (decoder logic circuits 35) are connected through a **polysilicon conductor layer** to the power transistors (FET drive circuits 85). Ex. 1007 ¶¶ 88-95.

Figure 7 depicts "an electrical circuit schematic" showing the **FET drive circuit 85 (green) connected to the decoder logic circuit 35 (yellow)**. Ex. 1004 at 2:37; Ex. 1007 ¶ 89.



Ex. 1004 at Fig. 7.

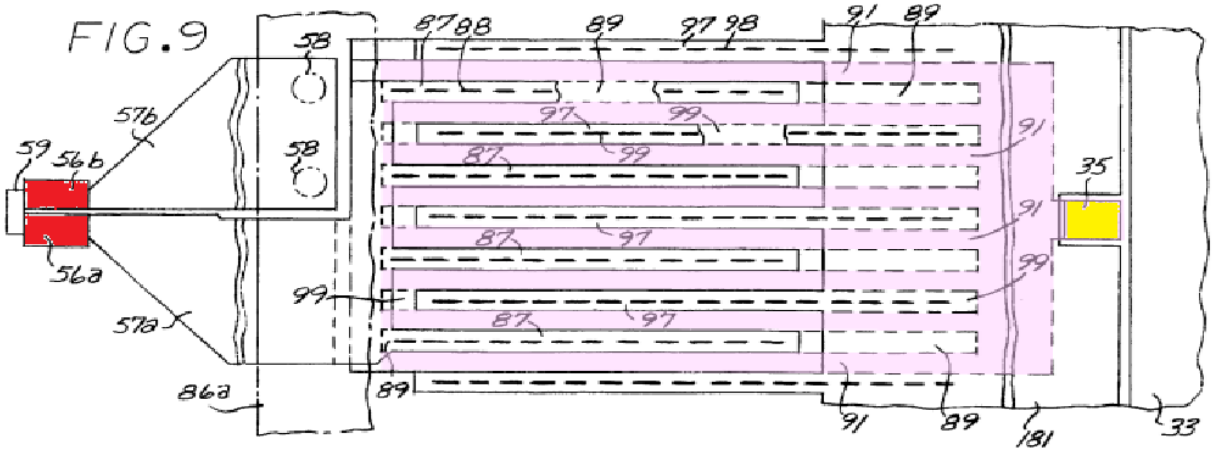
As seen in Figure 7, the FET drive circuit 85 (green) has three connections: (i) one to the heater resistor (56); (ii) one to the ground bus 181; and (iii) one **connecting the FET drive circuit 85 (green) to the decoder logic circuit 35 (yellow)**. Ex. 1004 at Fig. 7; Ex. 1007 ¶ 90. In other words, Figure 7 expressly shows that a connection exists between the FET drive circuits 85 and the decoder logic circuits 35. Ex. 1007 ¶ 91.

Figure 9 illustrates "a schematic plan view of an illustrative implementation of an **FET drive circuit** and a ground bus of the printheads of FIGS. 1A and 1B." Ex. 1004 at 2:42-44. Specifically, Figure 9 shows a more detailed drawing of the three connections to the FET drive circuits (85) from Figure 7, including how the FET drive circuit (85) connects to the decoder logic circuit (35). Ex. 1007 ¶¶ 89-92.

Torgerson explains:

> **[E]ach of the FET drive circuits 85 comprises** a plurality of electrically interconnected **drain electrode fingers 87** disposed over **drain region fingers 89** formed in the silicon substrate 111a (FIG. 5), and a plurality of electrically interconnected **source electrode fingers 97** interdigitated or interleaved with the **drain electrodes 87** and disposed over **source region fingers 99** formed in the silicon substrate 111a. **Polysilicon gate fingers 91 that are interconnected at respective ends** are disposed on a thin gate oxide layer 93 formed on the silicon substrate 111a. A phosphosilicate glass layer 95 separates the drain electrodes 87 and the source electrodes 97 from the silicon substrate 111a. A plurality of conductive drain contacts 88 electrically connect the drain electrodes 87 to the drain regions 89, while a plurality of conductive source contacts 98 electrically connect the source electrodes 97 to the source regions 99.

Ex. 1004 at 7:32-48.



Ex. 1004 at Fig. 9.

As discussed, Figure 7 illustrates a connection exists between the FET drive circuits (85) and the decoder logic circuits (35). Ex. 1007 ¶ 91; Ex. 1004 at Fig. 7. As seen in Figure 9, the only connection that exists between the **decoder logic circuit 35 (yellow) and the FET drive circuit 85** is the **polysilicon gate fingers 91 (pink) connecting the decoder logic circuit 35 to the FET drive circuit 85**. Ex. 1004 at Fig. 9; Ex. 1007 ¶ 93. As Torgerson explains, the FET drive circuit 85 comprises drain electrode fingers 87, drain region fingers 89, source electrode fingers 97, drain electrodes 87, and source region fingers 99, which are all individually labeled in Figure 9. Ex. 1004 at 7:32-39; Ex. 1007 ¶ 93.

Therefore, Torgerson discloses "a **columnar array of logic circuits** [e.g., columnar array 31 of decoder logic circuits 35 as seen in Fig. 6] disposed **adjacent the columnar array of power transistors** [e.g., columnar array 81 of FET drive circuits 85 as seen in Fig. 6] and connected through a **polysilicon conductor layer** [e.g., polysilicon fingers/gates 91 as seen in Fig. 9] to **the power transistors** [e.g., FET drive circuits 85 as seen in Fig. 9], the columnar array of logic circuits occupying a **logic circuit area of the substrate** [e.g., yellow box in annotated Figure 6 above]." Ex. 1007 ¶¶ 85-96.

Limitation 1[D] "a power conductor for the ejection actuators routed in a second metal conductor layer disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate":

Torgerson discloses this limitation. Ex. 1007 ¶¶ 97-105.

In Torgerson, the **primitive select traces 86a, 86b, 86c, 86d** correspond to the claimed power conductor for the ejection actuators (heater resistors 56). Ex. 1007 ¶ 99.

Torgerson explains that "the ink drop generators of a columnar array 61 of ink drop generators can be organized into four primitive groups 61a, 61b, 61c, 61d of contiguously adjacent ink drop generators, and the **heater resistors 56** of a particular primitive group are **electrically connected to the same one of four primitive select traces 86a, 86b, 86c, 86d**, such that the ink drop generators of a particular primitive group are switchably coupled in parallel to the same ink firing primitive select signal PS." Ex. 1004 at 5:44-52.

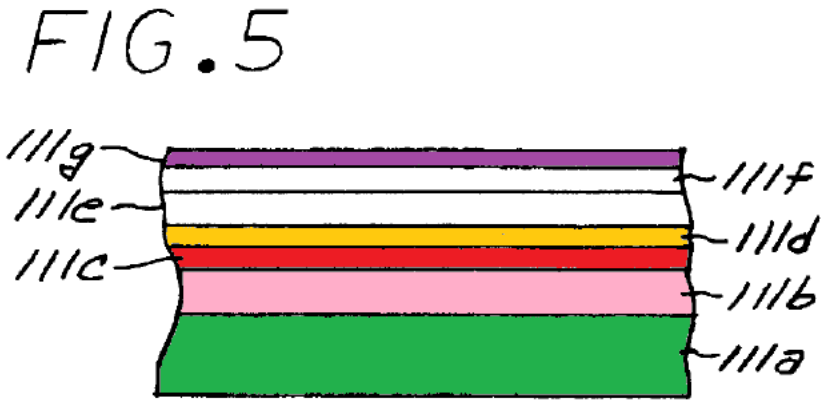
As explained by Torgerson, the primitive select traces 86a-86d are routed in a second metal conductor layer in overlapping relationship with at least a portion of the FET drive circuits 85. Ex. 1007 ¶¶ 100-104. Torgerson explains that the primitive select traces 86a-86d reside in the "**gold metallization layer 111g**" of the thin film substructure. Ex. 1004 at 5:59-64. This **gold metallization layer 111g** is the claimed second metal conductor layer and is disposed in overlapping relationship

with at least a portion of the power transistor active area of the substrate. Ex. 1007 ¶¶ 100-104

As Torgerson notes when describing the substructure 11 with respect to Figure 5:

> [A] silicon substrate 111a, an FET gate and dielectric layer 111b, a resistor layer 111c, and a first metallization layer 111d. Active devices such as **drive FET circuits described more particularly herein are formed in the top portion of the silicon substrate 111a [green] and the FET gate and dielectric layer 111b [pink] . . .** Thin film heater resistors are formed by the respective patterning of the resistor layer 111c [red] and the first metallization layer 111d [orange]. The thin film substructure 11 further includes a composite passivation layer 111e comprising for example a silicon nitride layer and a silicon carbide layer, and a tantalum mechanical passivation layer 111f **that overlies at least the heater resistors 56. A gold conductive layer 111g [purple] overlies the tantalum layer 111f**.

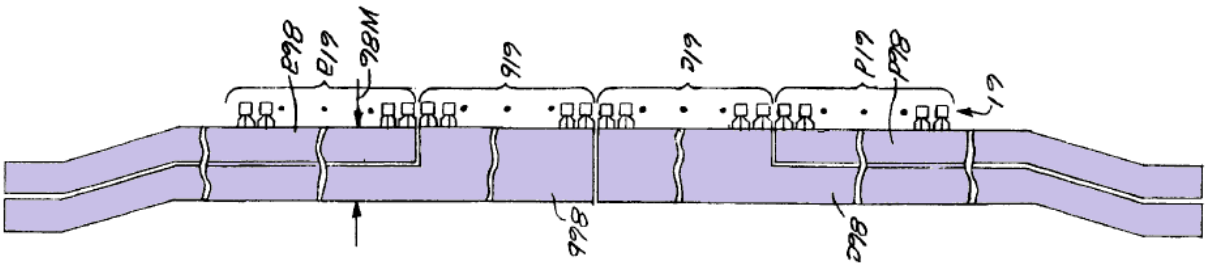
Ex. 1004 at 3:2-17.



Ex. 1004 at Fig. 5.

Thus, the gold metallization layer 111g (purple) in which the traces 86a-86d are formed overlies the layer in which the FET drive circuits 85 are formed (green and pink). Ex. 1007 ¶¶ 100-104. This gold metallization layer 111g (purple) is the "second metal conductor layer" with 111d (orange) described as the "first metallization layer." Ex. 1007 ¶¶ 82, 83, 100-104. Torgerson expressly describes the gold metallization layer 111g as a "conductive layer." Ex. 1004 at 3:16.

In describing Figure 8, Torgerson further notes that it shows "a schematic top plan view of **primitive select traces 86a, 86b, 86c, 86d [purple]** for an associated columnar array 61 of drop generators and an associated columnar array 81 of FET drive circuits 85 (FIG. 6) as implemented for example by **traces in the gold metallization layer 111g (FIG. 5) [purple] that is above and dielectrically separated from the associated array 81 of FET drive circuit**." Ex. 1004 at 5:59-65.



Ex. 1004 at Figs. 8.

Claim 13 of Torgerson also notes that the "M **primitive select traces overlie said columnar array of FET drive circuits**." Ex. 1004 at cl. 13. The M primitive select traces correspond to the claimed power conductor and thus overlap the FET drive circuits that occupy the power transistor active area. Ex. 1007 ¶ 102.

Therefore, Torgerson discloses "**a power conductor** [e.g., traces 86a, 86b, 86c, 86d] for the ejection actuators [e.g., heater resistors 56] routed in a **second metal conductor layer** [e.g., gold conductive layer 111g] disposed **in overlapping relationship** [e.g., Fig. 8] with at least a portion of the **power transistor active area** [e.g., yellow box in annotated Fig. 6 above] of the substrate."

Limitation 1[E] "a ground conductor for the ejection actuators routed in the second metal conductor layer disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate":

Torgerson in view of Bruce renders this limitation obvious. Ex. 1007 ¶¶ 106-114.

As described below, Torgerson discloses a ground conductor (ground bus 181) for the ejection actuators but fails to disclose the ground conductor being routed in the second metal conductor layer disposed in an overlapping relationship with at least a portion of the logic circuit area of the substrate.

Specifically, Torgerson discloses that "[a]ssociated with each FET drive circuit array 81 and **the associated array of ink drop generators is a columnar ground bus 181** to which the source electrodes of all of the FET drive circuits 85 of the associated FET drive circuit array 81 are electrically connected." Ex. 1004 at 5:6-10.

This **ground bus 181** corresponds to the claimed ground conductor. Ex. 1007 ¶ 108.

Although Torgerson does not teach placing its ground bus 181 in the second metal conductor layer (gold metallization layer 111g) disposed in an overlapping relationship with at least a portion of the logic circuit area of the substrate, this limitation is disclosed by Bruce. Ex. 1007 ¶¶ 109-112.

Bruce describes a "fluid ejection device [that] comprises a first metal layer and a second metallayer [*sic*]." Ex. 1005 at Abstract. Figure 1 shows "a block diagram of relative positions of metal portions of an exemplary embodiment of a fluid ejection device." Ex. 1005 at 1:32-34. In Figure 1, "[a] thin film stack comprises a first metal layer 1 and a **second metal layer 11**." Ex. 1005 at 2:65-66.

In Figure 1, **a ground conductor (ground portion 8, blue) is routed in the second layer of the substrate (11)** and overlaps the logic portion 5 (yellow) in the first layer. Ex. 1005 at Fig. 1, 5:55-63, 2:50-59; Ex. 1007 ¶¶ 110-111.

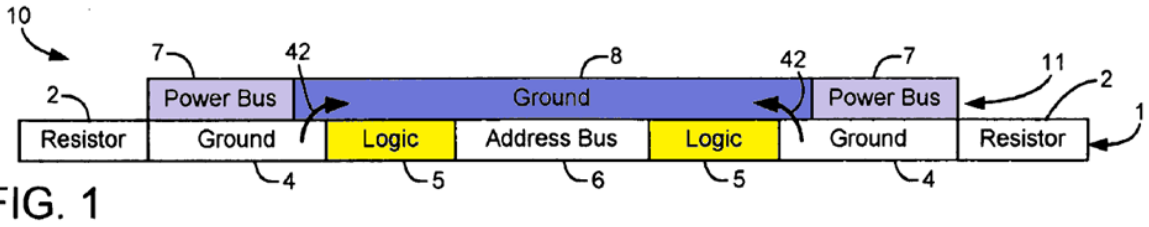


FIG. 1

Ex. 1005 at Fig. 1.

As discussed in more detail below, it would have been obvious for a PHOSITA to implement Bruce's second-metal-layer ground conductor in Torgerson and thus modify the ground bus (181) of Torgerson to place it largely in the second metal layer (gold conductive layer 111g) instead of the first metallization layer (111d). Ex. 1007 ¶ 112. Such placement in the second metal layer (gold conductive layer 111g) would place the ground bus (181) of Torgerson in overlapping relationship with at least a portion of the logic circuit area. *Id*. Such a modification would have been obvious because, as Bruce explains, placing a ground conductor in the second metal layer "avoids costs associated with increased die sizes" and "may result in reduced energy variation due to decreased ground resistance resulting from the greater ground area." Ex. 1005 at 2:50-59.

Therefore, Torgerson in view of Bruce discloses "a **ground conductor** [e.g., modify Torgerson's ground bus 181 to be like Bruce's ground portion 8 and in

second layer] for the **ejection actuators** [e.g., Torgerson's heater resistors 56] routed in the **second metal conductor layer** [e.g., Torgerson's gold conductive layer 111g] disposed in **overlapping relationship** [e.g., as in Fig. 1 of Bruce] with at least a portion of the **logic circuit area** [e.g., yellow box in annotated Fig. 6 of Torgerson above and logic 5 in Bruce Fig. 1] of the **substrate** [e.g., die 11 comprising a substrate such as silicon]." Ex. 1007 ¶¶ 106-114.

Motivation to Combine: Torgerson and Bruce

As explained above, Torgerson disclose all limitations of claim 1 except for placing a ground conductor in the second metal layer in overlapping relationship with at least a portion of the logic circuit area, but this limitation is disclosed by Torgerson in view of Bruce. It would have been obvious to implement Bruce's second-metal-layer ground conductor in Torgerson such that the ground bus of Torgerson was placed largely in the second metal layer in overlapping relationship with at least a portion of the logic circuit area for a number of reasons. Ex. 1007 ¶¶ 115-126.

***First*,** Torgerson and Bruce are **analogous art** to the claimed invention of the '341 Patent because they are all in the **same field of endeavor**—semiconductor substrates for an ink jet printhead—and **address the same problem**—decreasing the substrate size. Ex. 1007 ¶¶ 116-117. Indeed, the USPTO classified all three of these

patents under the same classification number: U.S. Cl. 347. Ex. 1001 at 1; Ex. 1004 at 1; Ex. 1005 at 1.

As the '341 Patent notes, it is directed to "[a] semiconductor substrate for a micro-fluid ejection device" and seeks to provide "improved conductor layouts for **reduced substrate size**." Ex. 1001 at Abstract, 1:6-8.

Like the '341 Patent, Torgerson is directed to ink jet printheads and specifically describes die 11 comprising a substrate such as silicon forming the semiconductor substrate for the printhead noting the "**need for an ink jet printhead that is compact**" and that "allows for a **narrower,** and thus less costly, thin film substructure." Ex. 1004 at Abstract, Figs. 1A-4A, 1B-4B, 1:59-63, 2:57-3:1, 8:48-56.

Like the '341 Patent and Torgerson, Bruce also describes the substrate of an ink jet printhead and seeks to decrease the size of the substrate explaining that its layout incorporating a ground portion in the second metal layer "**avoids costs associated with increased die sizes**." Ex. 1005 at Abstract, 1:6-23, 2:55-59, 3:55-59, Figs. 1, 10.

Moreover, Torgerson and Bruce have an overlapping inventor (Torgerson) and share the same assignee—Hewlett-Packard Development Company, L.P.

Second, a PHOSITA would have understood that supplementing Torgerson's ground bus (181) such that it is routed in the second metal conductor layer would

have been obvious because there are a finite number of identified, predictable solutions to reduce the substrate size of a printhead. Ex. 1007 ¶¶ 119-123. One identified, predictable option to reduce substrate size would be to reduce the area occupied by the ground bus. *Id*. ¶ 119. A PHOSITA would have understood that the ground bus must be placed in a metal layer in the substrate. *Id*.

To reduce the area occupied by the ground bus, a PHOSITA would have understood that two options exist. Ex. 1007 ¶ 120. A PHOSITA would have understood that he could make the first metal layer thicker and place the ground bus only in the first metal layer. *Id.* The increased thickness (i.e., height) of the first metal layer means a smaller width can be used to retain the same area occupied by the ground bus. *Id.* A smaller width would result in a smaller substrate. *Id.*

However, a PHOSITA would have understood that increasing the first metal layer's thickness (i.e., its height) would not have been a desired option because it would require that the dielectric and mechanical passivation of the heater resistor first metal connections cover substantially higher metal step heights. Ex. 1007 ¶ 121. Failure of the passivation at these heater resistor connection points is a primary failure mode for thermal inkjet devices. *Id*.

A PHOSITA would have thus understood that the second option available would have been to place a ground bus in the second metal layer, which is what Bruce discloses. Ex. 1007 ¶ 122; Ex. 1005 at Fig. 1. As the second metal layer does

not have the same circuitry (e.g., power transistors, logic) as the first metal layer, a PHOSITA would have understood that the ground bus can occupy a wider space in the second metal layer than what is available to it in the first metal layer without having to increase the width of the substrate itself. Ex. 1007 ¶ 122.

Because Bruce teaches placement of the ground portion (8) in the second metal layer as one identified solution to decrease substrate size, Ex. 1005 at 2:55-59, 3:55-59, modifying Torgerson to also have a ground bus (181) in the second metal layer would have been a predictable variation. Ex. 1007 ¶ 123.

Third, a PHOSITA would have been motivated to combine Torgerson with Bruce and supplement the ground bus (181) of Torgerson in the second metal conductor layer (111g) based on Bruce's teachings. Ex. 1007 ¶ 124. Torgerson and Bruce each describe placing the power conductor portion in overlapping relationship with at least a portion of the power transistor active area, which a PHOSITA would have understood helps reduce substrate size. *See* Section IX.A.1; Ex. 1005 at Figs. 3-4, 3:33-40, 4:18-24, 4:62-65; Ex. 1007 ¶¶ 97-105.

Bruce also explains that by placing a ground portion (8) in the second metal layer (11) of the printhead substrate, this yields certain advantages including: (i) "**reduced energy variation** due to decreased ground resistance resulting from the greater ground area"; (ii) "**avoids costs** associated with increased die sizes which result where ground resistance is decreased by widening ground paths in the first

metal layer, with corresponding increases in the die size"; and (iii) "**increase[s]** the **improvements in energy variation** that can be achieved by increasing the thickness of the second metal layer 11." Ex. 1005 at 2:50-63.

Because Torgerson and Bruce seek to address an overlapping problem—reducing the substrate size—and Bruce expressly teaches that by running a ground portion (8) in the second metal layer overlying at least a portion of the logic circuit area of the substrate it decreases substrate size, a PHOSITA would have been motivated to modify Torgerson to also have its ground bus (181) in the second metal layer and in overlapping relationship with the logic circuit area. Ex. 1007 ¶ 126.

2. Claim 2

Claim 2 requires "[t]he semiconductor substrate of claim 1, wherein the **fluid ejection actuators comprise heater resistors**," which is disclosed by Torgerson. Ex. 1007 ¶¶ 127-129.

As discussed in IX.A.1, limitation (A), incorporated herein, Torgerson uses **heater resistors 56**. *See, e.g.*, Ex. 1004 at 3:38-4:5.

Therefore, Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the **fluid ejection actuators comprise heater resistors** [e.g., heater resistors 56]." Ex. 1007 ¶¶ 127-129.

3. Claim 3

Claim 3 requires "[t]he semiconductor substrate of claim 1, wherein the semiconductor substrate contains **at least three fluid supply slots** and associated ejection actuators, power transistors, logic circuits, and conductors," which Torgerson discloses. Ex. 1007 ¶¶ 130-136.

As discussed in IX.A.1, limitation (A), incorporated herein, Torgerson explains that the "thin film substructure 11 of the printhead 100A of FIGS. 1A, 2A, 3A, 4A more particularly includes **three ink feed slots 71**." Ex. 1004 at Fig. 4A, 4:36-40.

As seen in Figure 4A, each ink feed slot (71, brown) is associated with its own columnar array of heater resistors (56, red). Ex. 1004 at Fig. 4A, 3:66-4:5, 4:40-48; Ex. 1007 ¶ 132. Torgerson explains that "[i]nsofar as each of the ink drop generators 40 includes a heater resistor 56, the heater resistors are accordingly arranged in columnar groups or arrays that correspond to the columnar arrays of ink drop generators." Ex. 1004 at 4:29-32.

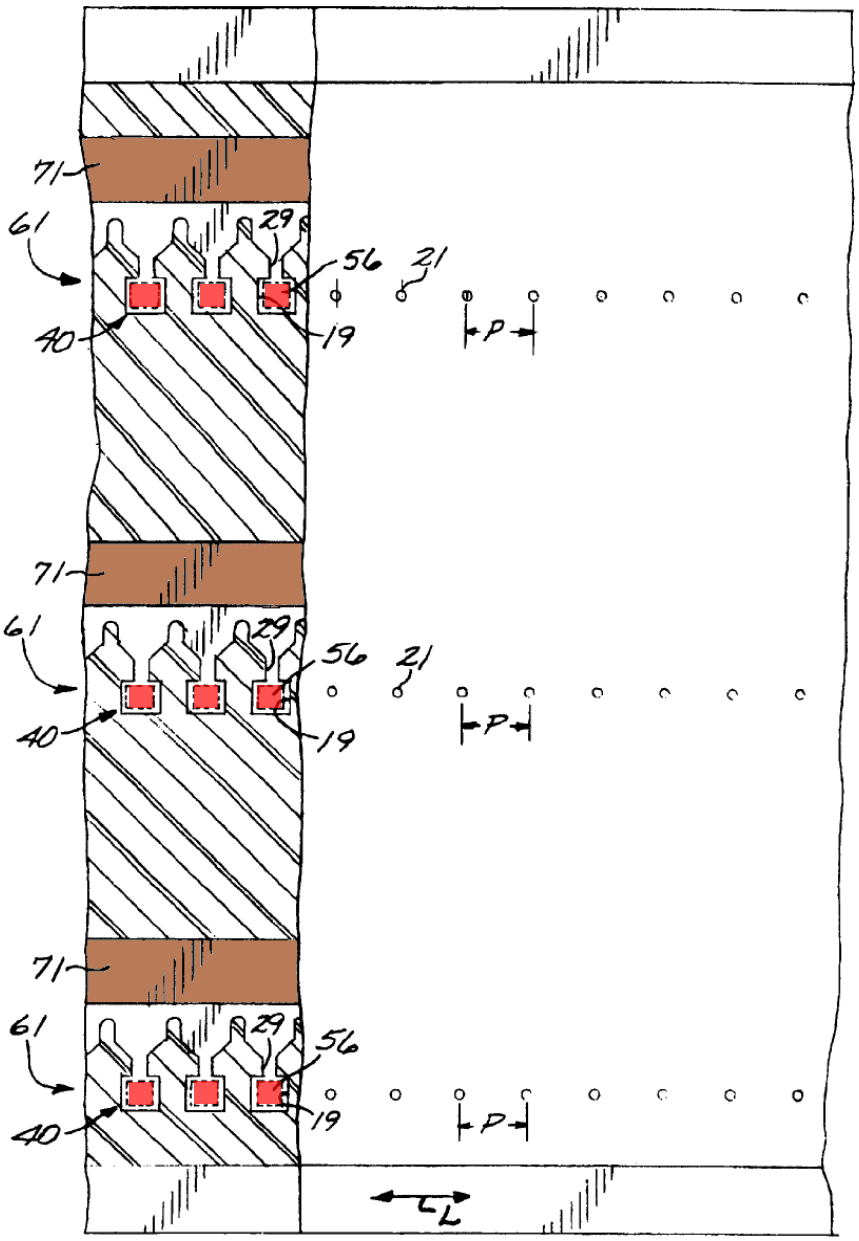


FIG.4A

Ex. 1004 at Fig. 4A.

As Torgerson explains, "adjacent and associated with the columnar arrays 61 of ink drop generators 40 are columnar FET drive circuit arrays 81" with each "FET drive circuit array 81 includ[ing] **a plurality of FET drive circuits 85** having drain

electrodes respectively connected to respective heater resistors 56 by heater resistor leads 57a." Ex. 1004 at 4:65-5:6. Torgerson further explains that associated "with each FET drive circuit array 81 and the associated array of ink drop generators is a **columnar ground bus 181**," and the "FET drive circuits 85 of each columnar array of FET drive circuits are controlled by **an associated columnar array 31 of decoder logic circuits 35** that decode address information on an adjacent address bus 33." Ex. 1004 at 5:6-10, 24-28. Torgerson also notes that "the heater resistors 56 of a particular primitive group are electrically connected to the same one of four **primitive select traces 86a, 86b, 86c, 86d**." Ex. 1004 at 5:42-51.

A PHOSITA would have therefore understood that each ink feed slot 71 of Torgerson has its own columnar array of heater resistors (56), FET drive circuits (85), logic decoder circuits (35), and power (86a-86d) and ground (bus 181) conductors.[5] Ex. 1007 ¶¶ 130-136.

Therefore, Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the semiconductor substrate [e.g., substructure 11] contains **at least three fluid supply slots** [e.g., ink feed slots 71] and associated **ejection actuators** [e.g.,

[5] Note the ground bus 181 of Torgerson associated with each ink feed slot 71 would have been modified in view of Bruce as described in Section IX.A.1, limitation [E], incorporated herein.

heater resistors 56], **power transistors** [e.g., FET drive circuits 85], **logic circuits** [e.g., decoder logic circuits 35], and **conductors** [e.g., traces 86a, 86b, 86c, 86d as the power conductor and ground bus 181 of Torgerson as modified by Bruce's teaching of ground portion 8 as discussed in Section IX.A.1 as the ground conductor]." Ex. 1007 ¶¶ 130-136.

4. Claim 4

Claim 4 requires "[t]he semiconductor substrate of claim 1, wherein the **power transistors comprise field effect transistors (FETS)**," which Torgerson discloses. Ex. 1007 ¶¶ 137-139.

As discussed in Section IX.A.1, limitation [B], incorporated herein, the power transistors in Torgerson are FET drive circuits 85 wherein FET stands for Field Effect Transistor. Ex. 1007 ¶ 138.

Therefore, Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the **power transistors comprise field effect transistors (FETS)** [e.g., FET drive circuits 85]." Ex. 1007 ¶¶ 137-139.

5. Claim 5

Claim 5 requires "[t]he semiconductor substrate of claim 1, wherein the **logic circuits** comprises [*sic*] circuits selected from the group consisting of **primitive address logic**, **predrive circuits,** data registers, and combinations of two or more of the foregoing," which Torgerson discloses. Ex. 1007 ¶¶ 140-144.

As discussed in Section IX.A.1, limitation [C], incorporated herein, the decoder logic circuits 35 of Torgerson are the claimed logic circuits. Torgerson explains "[t]he FET drive circuits 85 of each columnar array of FET drive circuits are controlled by an associated columnar array 31 of **decoder logic circuits 35 that decode address information** on an adjacent address bus 33 that is connected to appropriate bond pads 74 (FIG. 6)." Ex. 1004 at 5:24-28.

A PHOSITA would have understood that the decoder logic circuits 35 necessarily include at least **primitive address logic** since such circuits are needed to utilize the logic voltage states present on the address lines stemming from the limited number of bond pads 74. Ex. 1007 ¶ 142. A PHOSITA would have understood that the large number of drop generators cannot be individually addressed by individual bond pads. *Id*. Instead, at least **primitive address logic circuitry** would be included in the decoder logic circuits 35 associated with each FET drive circuit 85 to monitor the logic states on a limited number of address lines. *Id*. This necessary drop generator selection circuitry of the decoder logic circuits corresponds to the claimed **primitive address logic**. *Id*.

Torgerson also explains "[t]he address information identifies the ink drop generators that are to be energized with ink firing energy, as discussed further herein, and is utilized by the decoder logic circuits 35 to **turn on the FET drive circuit of an addressed or selected ink drop generator**." Ex. 1004 at 5:28-32.

A PHOSITA would have understood that to "turn on the FET drive circuit of an addressed or selected ink drop generator" would require **predrive circuits** in the decoder logic circuits 35. Ex. 1007 ¶ 143.

Therefore, Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the **logic circuits** [e.g., logic decoder circuits 35] comprises [*sic*] circuits selected from the group consisting of **primitive address logic**, **predrive circuits,** data registers, and combinations of two or more of the foregoing." Ex. 1007 ¶¶ 140-144.

6. Claim 8

Claim 8 requires "[a] **micro-fluid ejection head** comprising the substrate of claim 1," which Torgerson discloses. Ex. 1007 ¶¶ 145-152.

A PHOSITA would have understood that the '341 Patent uses the term "micro-fluid ejection head" interchangeably with the term "micro-fluid ejection device." Ex. 1007 ¶¶ 147-150. A PHOSITA would have understood the term "micro-fluid ejection head" to refer to an ink jet printhead as those terms are used interchangeably in the art. Ex. 1007 ¶¶ 147-150.

As discussed in Section IX.A.1, preamble, incorporated herein, Torgerson discloses the substructure 11 being part of printhead 100A. Ex. 1004 at 2:57-61.

Therefore, Torgerson discloses "[a] **micro-fluid ejection head** [e.g., printhead 100A] comprising the substrate of claim 1 [e.g., die 11 comprising a substrate such as silicon]." Ex. 1007 ¶¶ 145-152.

B. Ground #2: Claims 1-5 and 8 are rendered obvious by Furukawa and Torgerson

1. Claim 1

Preamble 1[P] "A semiconductor substrate for a micro-fluid ejection device":

As discussed in Section IX.A.1, incorporated herein, the recitation in the preamble requiring "for a micro-fluid ejection device" is not limiting because it merely recites the intended use of the purported invention.

Even if limiting, Furukawa discloses this limitation. Ex. 1007 ¶¶ 155-162.

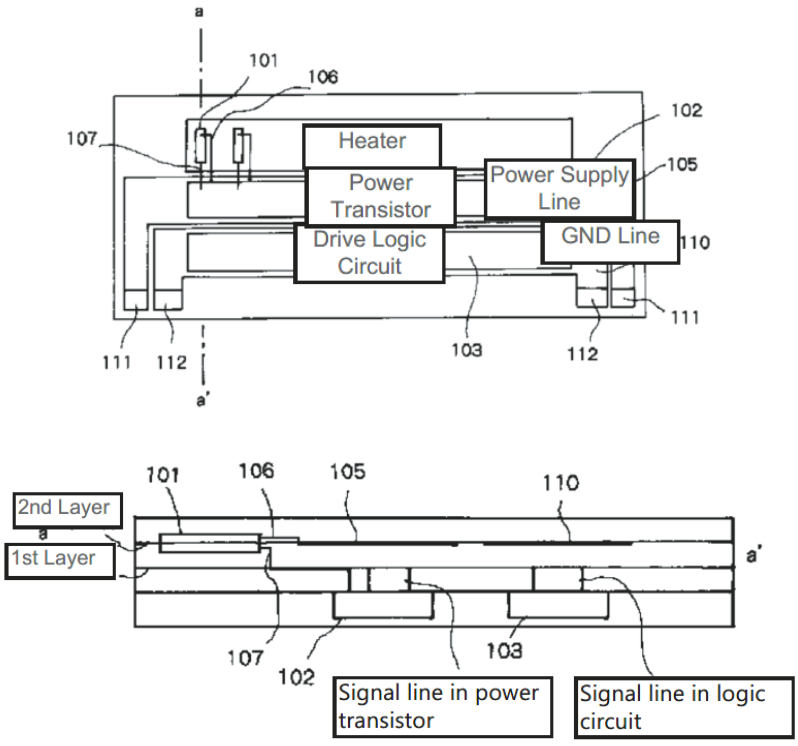
In particular, the **board depicted in Figures 3-4** of Furukawa corresponds to the claimed semiconductor substrate, which is included in the **recording head IJH** that corresponds to the claimed micro-fluid ejection device. Ex. 1007 ¶¶ 155-162.

Furukawa explains that the invention "concerns a recording head and a recording device using the recording head, and in particular, concerns a recording head and a recording device using the **recording head** which employs the **inkjet method** to record on recording media by discharging ink." Ex. 1006 at [0001].

Furukawa further explains that Figure 3 of Furukawa shows "the layout of each configuring component **mounted on the recording head IJH drive circuit**

board" and explains that "[t]his drive circuit board uses **multilayer wiring technology**, and the Al (aluminum or alloy containing aluminum) wiring connecting the configuring components has a multilayer structure **on the board**." Ex. 1006 at [0021].

Figure 4 of Furukawa illustrates "a section view of **the circuit board** along line a-a' indicated in Figure 3." Ex. 1006 at [0021]. A PHOSITA would have understood that this **board depicted in Figures 3-4** corresponds to the semiconductor substrate. Ex. 1007 ¶ 160.



Ex. 1006 at Figs. 3-4.

This board is "**mounted on the recording head IJH**," which corresponds to the claimed "micro-fluid ejection device." Ex. 1006 at [0021]; Ex. 1007 ¶ 161. A PHOSITA would have understood that the term "micro-fluid ejection device" is synonymous with Furukawa's recording head IJH. Ex. 1007 ¶ 161. Furukawa explains that "the recording head IJH [is] **mounted on the inkjet printer** IJRA." Ex. 1006 at [0020]. The '341 Patent notes "[m]icro-fluid ejection devices continue to be used in a wide variety of applications, including **ink jet printers**." Ex. 1001 at 1:12-13.

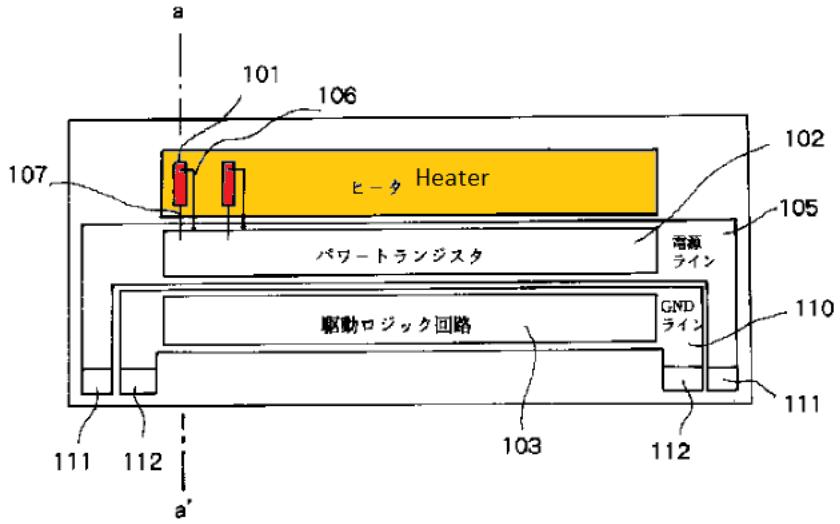
Therefore, Furukawa discloses "**[a] semiconductor substrate** [e.g., board in Figs. 3-4] for a **micro-fluid ejection device** [e.g., recording head IJH]." Ex. 1007 ¶¶ 155-162.

Limitation 1[A] "a plurality of micro-fluid ejection actuators disposed in a columnar array adjacent a fluid supply slot in the semiconductor substrate":

Furukawa as modified by Torgerson discloses this limitation. Ex. 1007 ¶¶ 163-171.

Furukawa teaches each of the elements of this limitation except for the fluid supply slot. Like the '341 Patent, Furukawa utilizes a plurality of **heaters 101** as the claimed plurality of micro-fluid ejection actuators that are disposed in a columnar array. Ex. 1007 ¶¶ 164-166; *see also* Ex. 1001 at 3:54-55 ("Ejection actuator 26 is **preferably a heater resistor**.").

As Furukawa explains, the recording head in the present invention comprises "a plurality of **thermoelectric conversion elements**." Ex. 1006 at [0013]. The thermoelectric conversion elements are **heaters (101)** shown in red below in Figure 3. Ex. 1006 at [0023]. As seen in Figure 3, there are a plurality of **heaters (101) (red)** disposed in a columnar array.



Ex. 1006 at Fig. 3.

Furukawa explains in relation to the conventional recording head's heater (401) that it "generates the heat required to discharge ink, and ink appropriate for the image data is discharged from the recording head nozzle." Ex. 1006 at [0006]. A PHOSITA would have understood that the heater (101) in Figure 3 performs the same function of generating "heat required to discharge ink" such that ink may be "discharged from the recording head nozzle." *Id.*; Ex. 1007 ¶ 166.

To the extent the Board determines that Furukawa does not disclose a "plurality of micro-fluid ejection actuators disposed in a columnar array" Torgerson discloses a columnar array of micro-fluid ejection actuators (columnar array 61 of heater resistors 56) as described in Section IX.A.1, incorporated herein. *See also* Ex. 1007 ¶ 166.

Figure 3 of Furukawa does not depict the recording head nozzles or the means by which ink is supplied to the recording head for discharge. Ex. 1007 ¶ 167. A PHOSITA would have understood that one well-known method for supplying ink to a recording head would be the use of fluid supply slot(s) such as those described in Torgerson. Ex. 1007 ¶¶ 167, 218.

Torgerson describes a substrate (die 11 comprising a silicon substrate) for an ink jet printhead (printhead 100A) that includes **three ink feed slots 71 (brown)** placed adjacent a columnar array of **heater resistors 56 (red)**. Ex. 1004 at Fig. 4A, 3:66-4:5, 4:36-45.

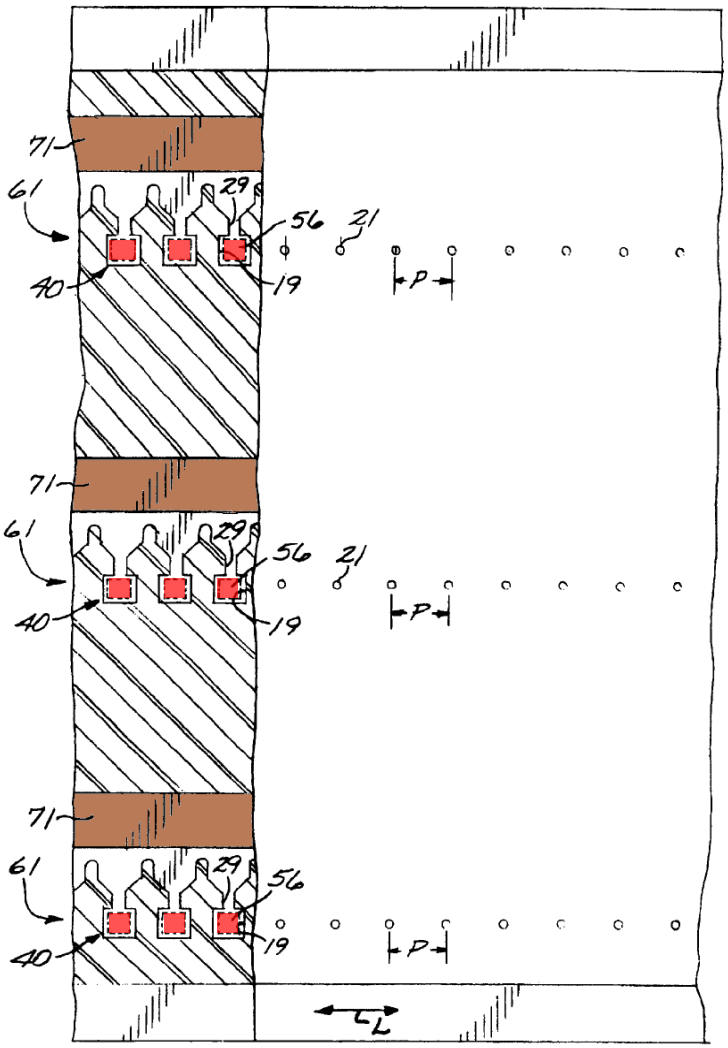


FIG.4A

Ex. 1004 at Fig. 4A.

As discussed in more detail below, it would have been obvious for a PHOSITA to implement Torgerson's three ink feed slots (71) in Furukawa to place each ink feed slot adjacent its own plurality of heater resistors (101). Ex. 1007 ¶ 170. Such a modification would have been obvious because, as Torgerson explains, having three ink feed slots allows for the provision of "ink of a color that is different

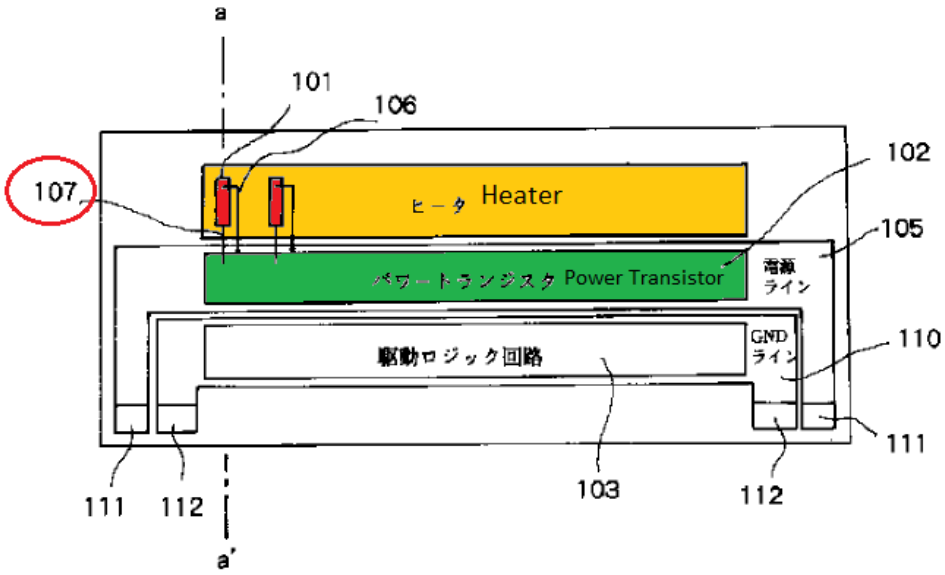
from the color of the ink provided by the other ink feed slots, such as cyan, yellow, and magenta." Ex. 1004 at 4:43-48.

Therefore, Furukawa in view of Torgerson discloses "a **plurality of micro-fluid ejection actuators** [e.g., Furukawa's heaters 101 or heater resistors 56 of Torgerson] disposed in a **columnar array** [e.g., Furukawa's Fig. 3 or array 61 of Torgerson] adjacent a **fluid supply slot** [e.g., Torgerson's ink feed slots 71] in the **semiconductor substrate** [e.g., Furukawa's Figs. 3-4]." Ex. 1007 ¶¶ 163-171.

Limitation 1[B] "a plurality of power transistors disposed in a columnar array adjacent the ejection actuators and connected through a first metal conductor layer to the ejection actuators, the columnar array of power transistors occupying a power transistor active area of the substrate":

Furukawa discloses this limitation. Ex. 1007 ¶¶ 172-187.

In Figure 3 of Furukawa, "**102 [green] is a power transistor**" and "107 [red circle] is wiring connecting the heater 101 [red] and the power transistor 102 [green]." Ex. 1006 at [0023-0024]. As seen in Figure 3, the heaters (101, red) are placed adjacent to the **power transistor (102, green)**.

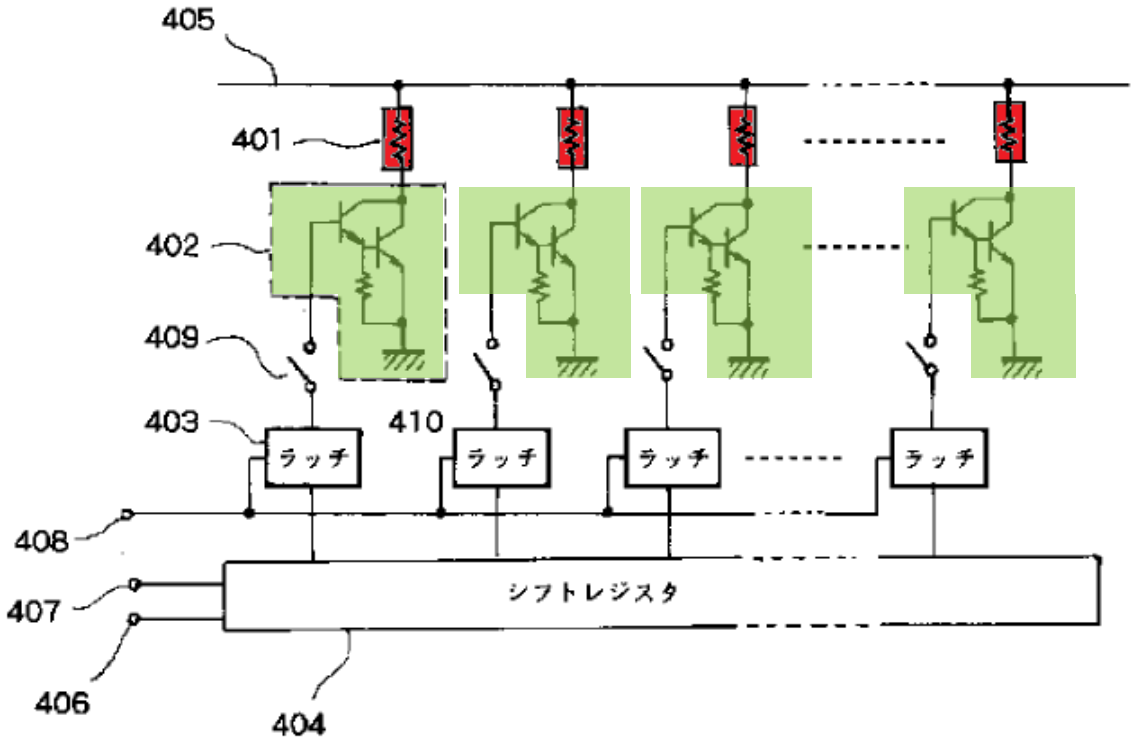


Ex. 1006 at Fig. 3.

Although Furukawa does not individually diagram individual power transistors in a columnar array within the green rectangular box labeled 102, a PHOSITA reading Furukawa would have understood that the rectangular green box 102 for the power transistors is a short-hand depiction of a columnar array of these power transistors for a number of reasons. Ex. 1007 ¶¶ 174-181.

First, in Figure 3, a plurality of heaters (101, red) are depicted with Furukawa explaining that "107 [red circle] is wiring connecting the heater 101 [red] and the power transistor 102 [green]." Ex. 1006 at [0024]." In Figure 3, an individual wire 107 emanates from each of the two depicted heaters (101, red) thus indicating to a PHOSITA that there are two separate power transistors present in box 102 (green)—one for each heater—that like the heaters (101) would also be placed in a similar columnar array. Ex. 1007 ¶ 175.

Second, the description in Furukawa of conventional recording heads in Figure 6 explains that "401 is a thermoelectric conversion element (heater) [red] for generating thermal energy, **402 is a power transistor portion [green]** for supplying a desired current to the heater 401." Ex. 1006 at [0002].

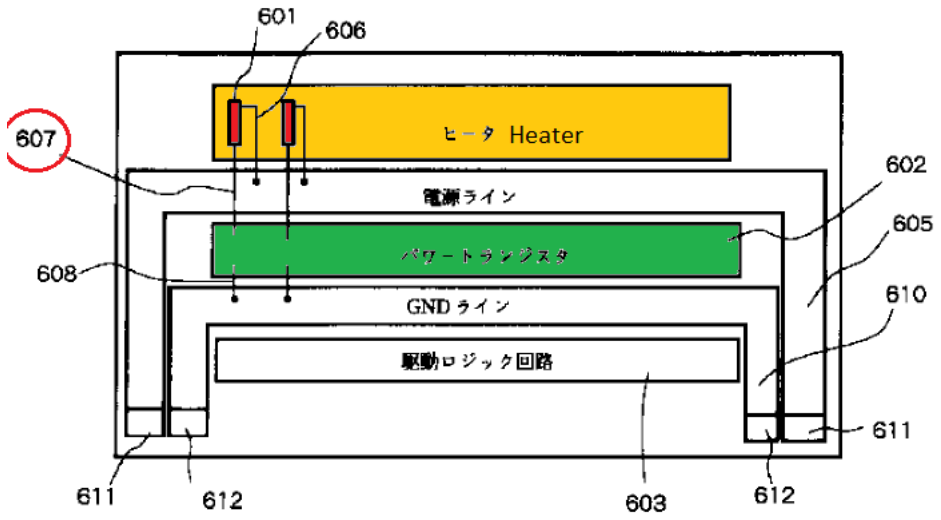


Ex. 1006 at Fig. 6.

As seen in Figure 6, the plurality of power transistors (402, green) is placed in a columnar array adjacent the heaters (401, red). A PHOSITA would have understood that this same layout of a columnar array of power transistors would have been utilized in the layout in Figure 3 because each heater (101) in Figure 3 must have its own associated power transistor. Ex. 1007 ¶ 177.

Third, a PHOSITA reviewing Figures 6 and 8 depicting the conventional recording heads would have understood that Furukawa utilizes the rectangular boxes in Figure 3 to short-hand depict the plurality of power transistors present in the substrate. Ex. 1007 ¶¶ 178-181.

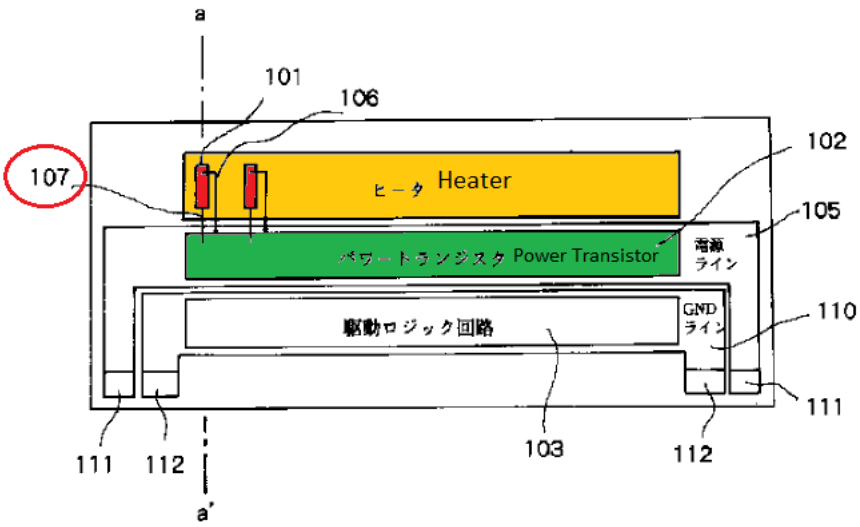
Despite depicting a columnar array of power transistors (402) in Figure 6, Furukawa depicts these as a sole rectangular box in Figure 8 noting that "Figure 8 is a drawing indicating the **layout when forming the drive circuit of a conventional recording head indicated in Figure 6 onto the same board**." Ex. 1006 at [0007].



Ex. 1006 at Fig. 8.

In Figure 8, 601 is a heater [red], **602 is a power transistor** [green]. . . , and 607 is wiring formed by Al wiring in the second layer and for **connecting the heater 601 and the power transistor 602**." Ex. 1006 at [0007].

As seen in Figure 8, although the detailed layout provided in Figure 6 depicts a plurality of power transistors (402, green) placed in a columnar array adjacent the plurality of heaters (401, red), the shorthand version used in Figure 8 depicts the plurality of power transistors by using a rectangular box (602, green). This same shorthand is used in Figure 3 of Furukawa where the power transistors 102 are depicted by the rectangular box labeled 102 (green).



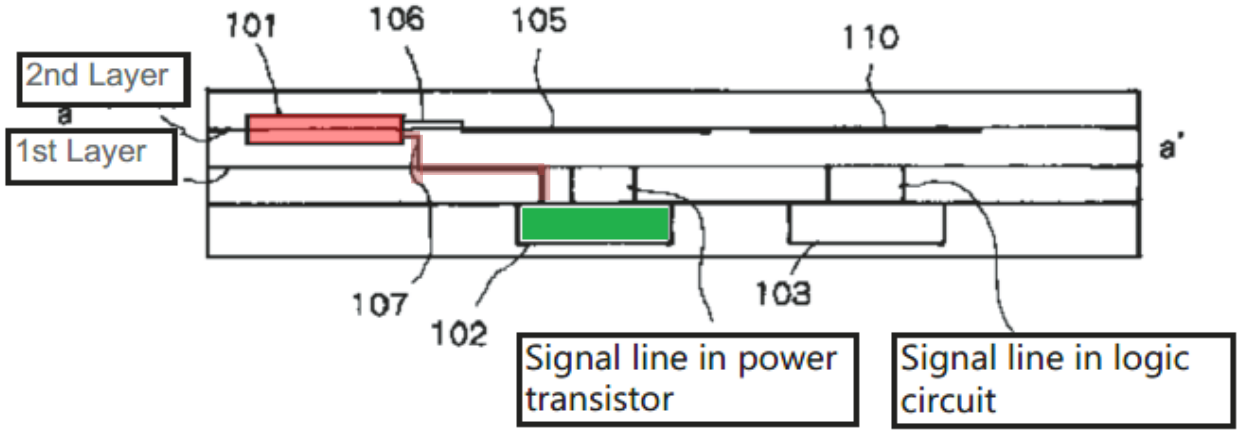
Ex. 1006 at Fig. 3.

Thus, a PHOSITA would have understood that in Figure 3 of Furukawa, there is a plurality of power transistors placed in a columnar array with each power transistor connected to a respective heater (101). Ex. 1007 ¶ 182. As in the '341 Patent, the area occupied by the columnar array of power transistors (as depicted in shorthand by the box labeled 102 in green) forms the **power transistor active area** of the substrate. Ex. 1007 ¶ 182; *see also* Ex. 1001 at 1:48-49 ("The columnar array of power transistors occupies a **power transistor active area** of the substrate.").

To the extent the Board determines that Furukawa does not disclose "a plurality of power transistors disposed in a columnar array," Torgerson discloses placing a plurality of power transistors (FET drive circuits 85) in a columnar array (81) adjacent a plurality of micro-fluid ejection actuators (heater resistors 56) as described in Section IX.A.1, incorporated herein. *See also* Ex. 1007 ¶ 183.

Claim 1 also requires that the plurality of power transistors be connected through a first metal conductor layer to the ejection actuators, which Furukawa discloses. Furukawa explains that "107 is wiring connecting the heater 101 and the power transistor 102, and is formed of **Al [aluminum] wiring in the first layer**." Ex. 1006 at [0024].

As seen in Figure 4, the heater 101 (red) is connected to the power transistor 102 (green) via wiring 107 (orange) formed in the first layer.



Ex. 1006 at Fig. 4.

Although Furukawa does not expressly state the first layer is a "conductor" layer, a PHOSITA would have understood that aluminum is a conductor. Ex. 1007 ¶ 186.

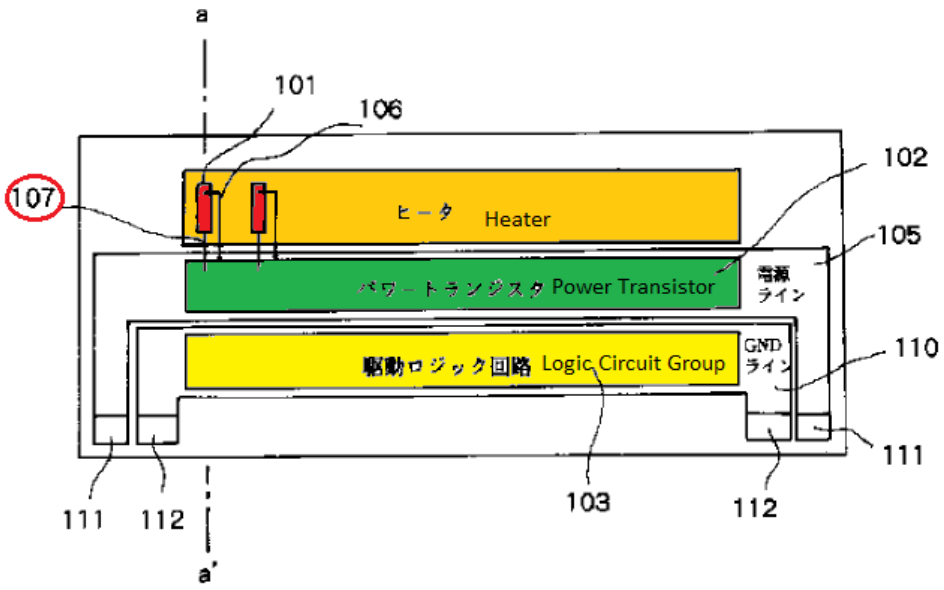
Therefore, Furukawa discloses "a **plurality of power transistors** [e.g., power transistor 102 in Furukawa or FET drive circuits 85 in Torgerson] disposed in a **columnar array** [e.g., box 102 in Fig. 3 in Furukawa or columnar array 81 in Torgerson] adjacent the **ejection actuators** [e.g., Furukawa's heaters 101 or heater resistors 56 of Torgerson] and connected through a **first metal conductor layer** [e.g., wiring 107 formed in first layer of Furukawa] to the ejection actuators, the columnar array of power transistors occupying a **power transistor active area** [e.g., green rectangle in Fig. 3 of Furukawa or yellow box in Fig. 6 of Torgerson in Section IX.A.1] of the substrate [e.g., Figs. 3-4 of Furukawa]." Ex. 1007 ¶¶ 172-187.

Limitation 1[C] "a columnar array of logic circuits disposed adjacent the columnar array of power transistors and connected through a polysilicon conductor layer to the power transistors, the columnar array of logic circuits occupying a logic circuit area of the substrate":

Furukawa as modified by Torgerson discloses this limitation. Ex. 1007 ¶¶ 188-202.

Furukawa discloses the elements of this limitation except the connection through the polysilicon conductor layer between the logic circuits and power

transistors. In Figure 3 of Furukawa, "**103 is a drive logic circuit group [yellow]** comprising a shift register, a latch circuit, a switch, etc." Ex. 1006 at [0023]. As seen in Figure 3, the logic circuit group 103 (yellow) is placed adjacent to the power transistor (102, green).



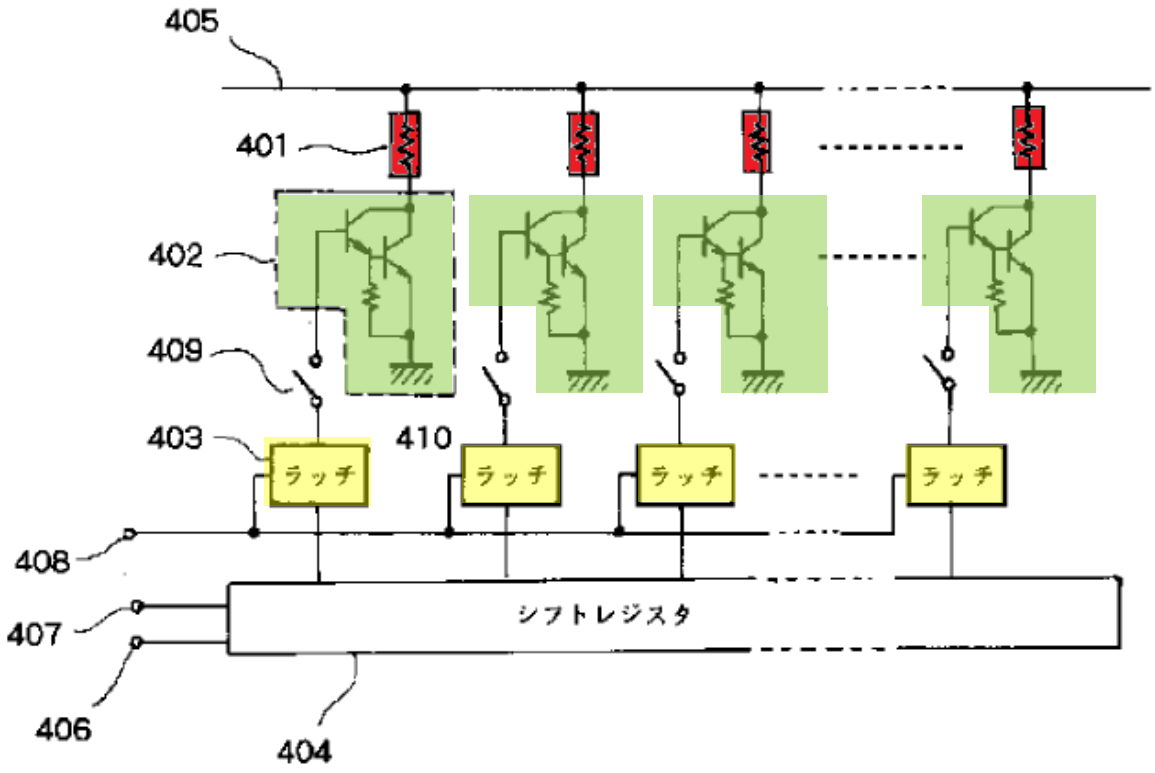
Ex. 1006 at Fig. 3.

As with the power transistors described above, Furukawa does not individually depict the logic circuits implemented on the substrate. A PHOSITA, however, would have understood that the box 103 (yellow) is a short-hand depiction of the columnar array of logic circuits that would be present with an individual logic circuit utilized for each power transistor and associated heater (101, red). Ex. 1007 ¶¶ 190-198.

First, given the depiction of a plurality of heaters (101, red) in a columnar array with individual wires 107 emanating from each heater 101 to the power

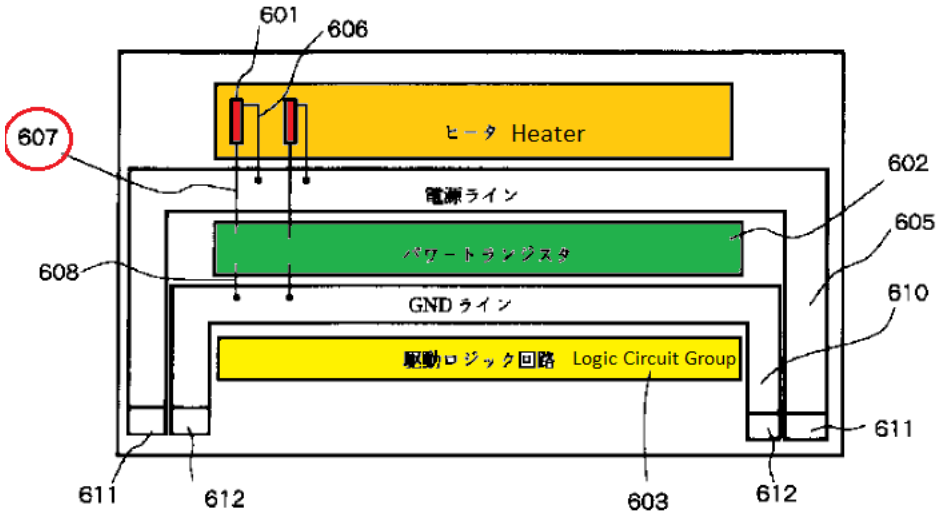
transistor box (102, green), a PHOSITA would have understood that each heater would have its own power transistor also placed in a columnar array, and each power transistor within box 102 (green) would likewise have its own logic circuit group in box 103 (yellow). Ex. 1007 ¶¶ 191.

Indeed, in Furukawa's depiction of a "conventional recording device," that each power transistor has its own logic circuit is clearly illustrated with 403 (yellow) being the latch circuit placed in a columnar array such that each power transistor (402, green) has its own latch circuit (403, yellow). Ex. 1006 at Fig. 6, p. 6 (Description of Fig. 6), [0002]; Ex. 1007 ¶¶ 191-193.



Ex. 1006 at Fig. 6.

Second, a PHOSITA reviewing Furukawa would have understood that Furukawa utilizes the rectangular boxes in Figure 3 as short-hand depictions of a plurality of elements. Ex. 1007 ¶ 194. This same short-hand is used in Figure 8, which is "a drawing indicating the **layout when forming the drive circuit of a conventional recording head indicated in Figure 6 onto the same board**." Ex. 1006 at [0007].



Ex. 1006 at Fig. 8.

In Figure 8, 601 is a heater [red], 602 is a power transistor [green], **603 is a driving logic circuit group [yellow]**." Ex. 1006 at [0007]. Although the detailed layout in Figure 6 depicts the logic circuits (403, yellow) in a columnar array, when depicted in Figure 8, it only shows a single rectangular box (603, yellow). This same shorthand is used in Figure 3 with the logic circuit group (103, yellow) also being depicted as a rectangular box.

Thus, a PHOSITA would have understood that in Figure 3 of Furukawa, there is a plurality of logic circuits with each logic circuit connected to a respective power transistor in the box 102 (green) and with the logic circuits placed in a columnar array. Ex. 1007 ¶ 198. As in the '341 Patent, the area occupied by the columnar array of logic circuits (as depicted in shorthand by the box labeled 103 in yellow) forms the **logic circuit area** of the substrate. Ex. 1007 ¶ 198; *see also* Ex. 1001 at 1:53-54 ("The columnar array of logic circuits occupies a **logic circuit area** of the substrate.").

To the extent the Board determines that Furukawa does not disclose "a columnar array of logic circuits disposed adjacent the columnar array of power transistors," Torgerson discloses a columnar array of logic circuits (columnar array 31 of decoder logic circuits 35) disposed adjacent the columnar array of power transistors (columnar array 81 of FET drive circuits 85) as described in Section IX.A.1, incorporated herein. *See also* Ex. 1007 ¶ 199.

Furukawa, however, does not disclose the connection between the power transistors and logic circuits as being through a polysilicon conductor layer. But, as described in detail above in Section IX.A.1, limitation [C], incorporated herein, Torgerson discloses connecting its FET drive circuits 85 and logic circuits on a substrate with polysilicon fingers (91, pink in Fig. 9 of Torgerson annotated above). Ex. 1004 at 2:42-46, 7:32-44, 8:48-53, Fig. 9.

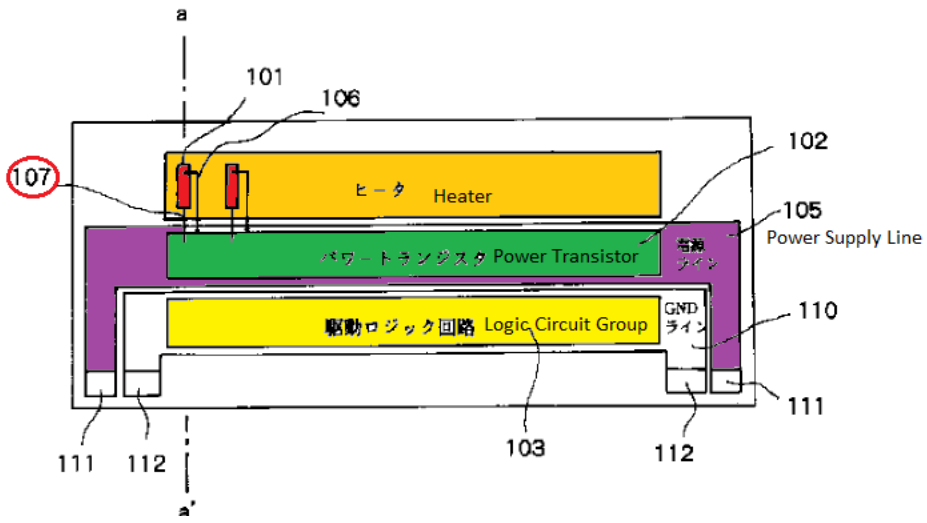
As discussed in more detail below, it would have been obvious for a PHOSITA to modify the substrate of Furukawa to utilize Torgerson's FET drive circuits (85) as the power transistors and then connect these to the logic circuits via the polysilicon connections described in Torgerson because a well-known advantage in the art of using FETs as the power transistors is that they provide better operational functions without requiring more space on the substrate. Ex. 1007 ¶ 201.

Therefore, Furukawa in view of Torgerson discloses "a **columnar array of logic circuits** [e.g., logic circuit group 103 of Furukawa or columnar array 31 of decoder logic circuits 35 of Torgerson] disposed **adjacent the columnar array of power transistors** [e.g., FET drive circuits 85 of Torgerson placed in position where 102 of Furukawa is located] and connected through a **polysilicon conductor layer** [e.g., Torgerson polysilicon gates 91] to the power transistors [e.g., FET drive circuits 85 of Torgerson placed in position where 102 of Furukawa is located], the columnar array of logic circuits occupying a **logic circuit area of the substrate** [e.g., 103 in Fig. 3 of Furukawa]." Ex. 1007 ¶¶ 188-202.

Limitation 1[D] "a power conductor for the ejection actuators routed in a second metal conductor layer disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate":

Furukawa discloses this limitation. Ex. 1007 ¶¶ 203-208.

In Furukawa, the **power supply line 105** corresponds to the claimed power conductor. Ex. 1007 ¶ 204. As seen in Figure 3, the **power supply line 105 (purple)** is disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate (102, green).

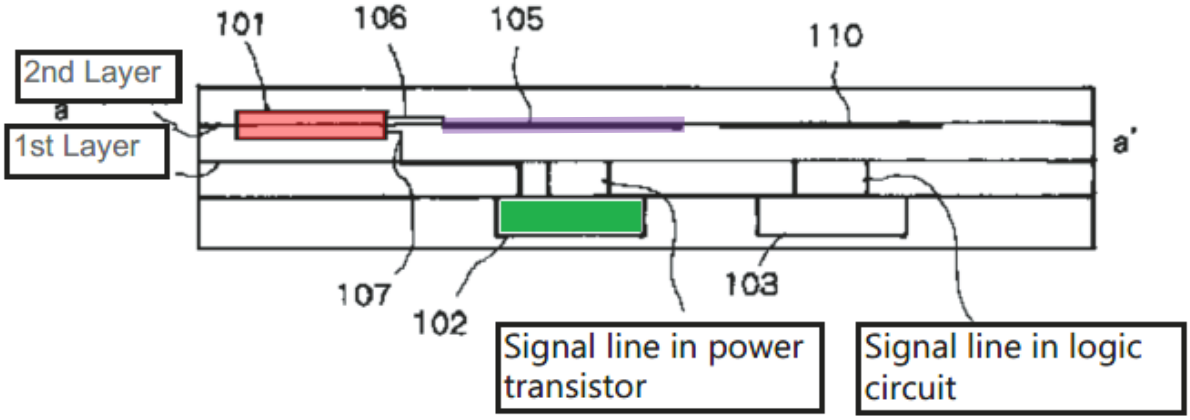


Ex. 1006 at Fig. 3.

As Furukawa explains, the power supply line 105 is "for applying a specified voltage across the heater 101" and "is positioned **on** the power transistor 102 element." Ex. 1006 at Fig. 3, [0023].

Furukawa also teaches that power supply line 105 (purple) is routed in a second metal conductor layer because it states "the **power supply line 105** is **formed** of Al (aluminum or alloy containing aluminum) wiring **in** the **second layer**." Ex. 1006 at [0023]. Although not expressly called a "conductor," a PHOSITA would have understood that as the second layer has aluminum wiring, it is a "conductor." Ex. 1007 ¶ 206.

Figure 4 depicts this illustrating the power supply line 105 (purple) in the second metal layer and overlapping the power transistor active area (102, green).



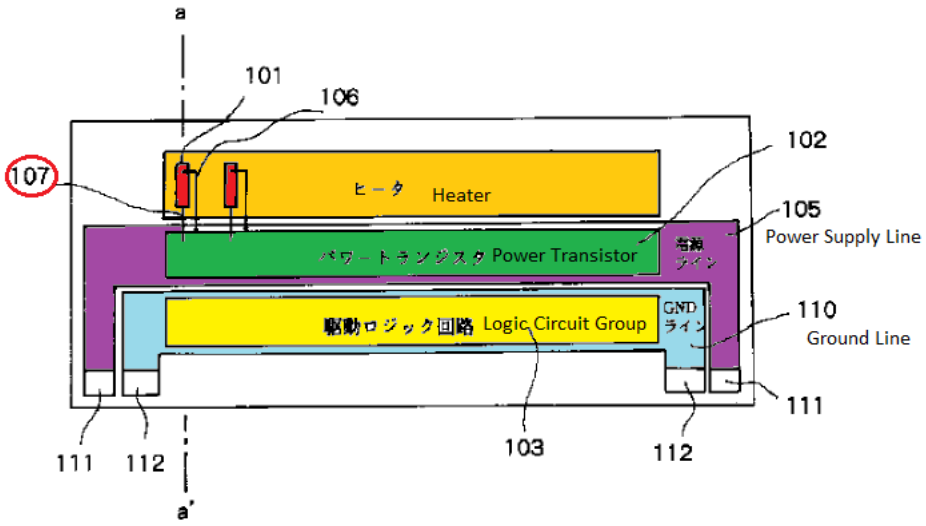
Ex. 1006 at Fig. 4.

Therefore, Furukawa discloses "**a power conductor** [e.g., power supply line 105] for the ejection actuators routed in a **second metal conductor layer** [e.g., Fig. 4] disposed **in overlapping relationship with at least a portion of the power transistor active area** [e.g., green box 102 in Fig. 3] of the substrate." Ex. 1007 ¶¶ 203-208.

Limitation 1[E] "a ground conductor for the ejection actuators routed in the second metal conductor layer disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate":

Furukawa discloses this limitation. Ex. 1007 ¶¶ 209-214.

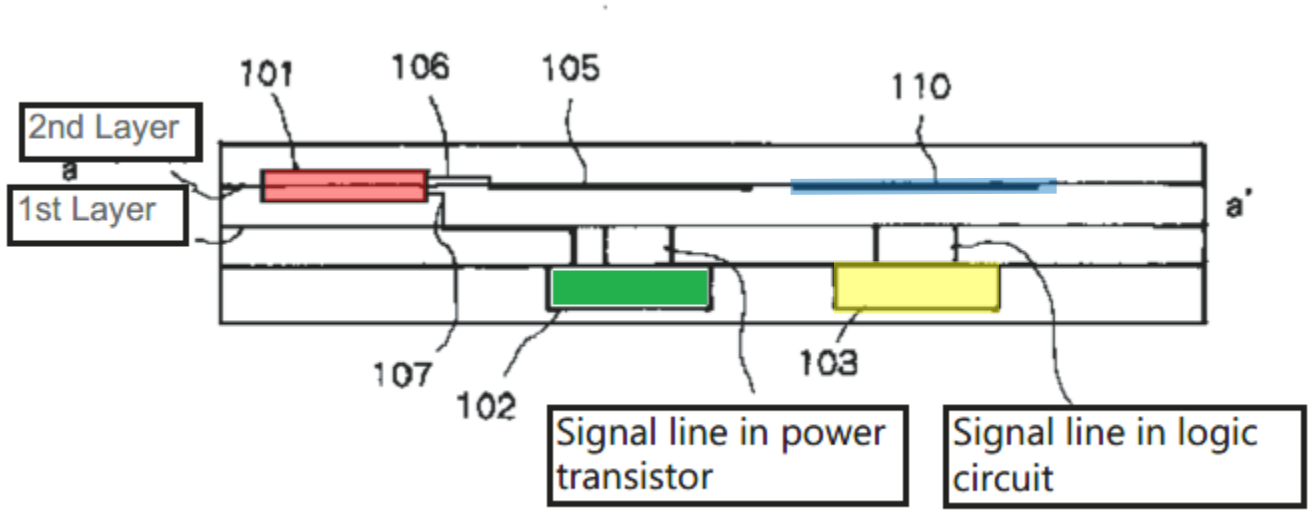
In Furukawa, **GND line 110** is the claimed ground conductor. Ex. 1007 ¶ 210. Furukawa explains that "**110 is a GND line [blue]** into which current from a power transistor 102 flows." Ex. 1006 at [0023].



Ex. 1006 at Fig. 3.

As seen in Figure 3, the GND line 110 (blue) is disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate (yellow box). Ex. 1006 at Fig. 3.

Furukawa also teaches that GND line 110 is routed in a second metal conductor layer because it states "the GND line 110 is **formed of Al wiring in the second layer**." Ex. 100 at [0026]. Figure 4 depicts the GND line 110 (blue) in the second metal layer and overlapping the logic area (103, yellow). Although not expressly called a "conductor," a PHOSITA would have understood that as the second layer has aluminum wiring, it is a "conductor." Ex. 1007 ¶ 212.



Ex. 100 at Fig. 4.

Therefore, Furukawa discloses "**a ground conductor** [e.g., GND line 110] for the ejection actuators routed in the **second metal conductor layer** [e.g., Fig. 4] disposed in **overlapping relationship** [e.g., Fig. 4] with at least a portion of the **logic circuit area** [e.g., yellow box 103 in Fig. 3] of the substrate." Ex. 1007 ¶¶ 209-214.

Motivation to Combine: Furukawa and Torgerson

As explained above, Furukawa disclose all limitations of claim 1 except for (i) a fluid supply slot placed adjacent the micro-fluid ejection actuators and (ii) a polysilicon connection between the power transistors and logic circuits, but these limitations are disclosed by Torgerson. It would have been obvious to a PHOSITA to modify Furukawa's substrate layout (Figs. 3-4) to incorporate fluid supply slots

adjacent the heaters (101) and to connect the power transistor and logic circuit of the substrate via a polysilicon conductor layer. Ex. 1007 ¶¶ 215-221.

***First*,** Furukawa and Torgerson are **analogous art** to the claimed invention of the '341 Patent because they are all in the **same field of endeavor**—semiconductor substrates for an ink jet printhead—and **address the same problem**—decreasing the substrate size. Ex. 1007 ¶ 216.

As the '341 Patent notes, it is directed to "[a] semiconductor substrate for a micro-fluid ejection device" and seeks to provide "improved conductor layouts for **reduced substrate size**." Ex. 1001 at Abstract, 1:6-8.

Like the '341 Patent, Furukawa describes a layout configuration for a substrate that can be used on a recording head of an ink jet printer and seeks to "**provide a more miniaturized recording head**." Ex. 1006 at [0012]. To achieve its objective, Furukawa approaches the layout in the same way as the '341 Patent by placing the power supply line and ground (GND) line in the second layer of the substrate and overlapping the power supply line and GND line with the power transistors and logic circuits, respectively. Ex. 1006 at [0021-0028], Fig. 3.

Like Furukawa and the '341 Patent, Torgerson is directed to ink jet printheads, and specifically describes the substructure or die (11) forming the semiconductor substrate for the printhead noting the "**need for an ink jet printhead that is compact**" and that "allows for a **narrower,** and thus less costly, thin film

substructure." Ex. 1004 at Abstract, Figs. 1A-4A, 1B-4B, 1:59-63, 2:57-3:1, 8:48-56.

Second, a PHOSITA would have understood that modifying Furukawa's layout of its board (substrate) to have three ink feed slots (71 in Torgerson) with each slot adjacent a plurality of heaters (101 in Furukawa) would have been obvious because means for supplying the ink to the recording head would have necessarily needed to be included so that the recording head could operate in the ink jet printer. Ex. 1007 ¶ 218. One well-known method for providing ink is to utilize fluid supply slots adjacent the heaters, as described by Torgerson such that this would have been an obvious design choice. Ex. 1004 at 4:36-48, Fig. 4A; Ex. 1007 ¶ 218.

Additionally, by utilizing three ink feed slots as described in Torgerson, this would allow for delivery of different colors of ink. Ex. 1007 ¶ 219. As Torgerson explains, "each of the ink feed slots provides ink of a color that is different from the color of the ink provided by the other ink feed slots, such as cyan, yellow and magenta." Ex. 1004 at 4:45-48.

A PHOSITA would have also been motivated to modify the board (substrate) of Furukawa to use Torgerson's FET drive circuits (85) as the power transistors and connect these power transistors to the logic circuit group of Furukawa via polysilicon connections. Ex. 1007 ¶ 220. Consistent with the goals of Furukawa, a well-known advantage in the art of using FETs is that they provide better operational functions

without requiring more space on the substrate. Ex. 1007 ¶¶ 220-221. Given that the '341 Patent and Furukawa seek to address the same problem of reducing the substrate size of the printhead, the utilization of FETs would be an obvious design choice to achieve that objective while also providing better operational functions to the substrate of Furukawa. *Id.* When FETs are used, those skilled in the art understand that it is common to connect the FETs to the logic groups via polysilicon, as described in Torgerson. Ex. 1007 ¶ 220.

Moreover, because these FET drive circuits of Torgerson are "configured to compensate for parasitic resistances of power traces," and the "area occupied by each FET drive circuits is preferably small, and the on-resistance of each FET drive circuit is preferably low," the smaller size of the circuits and compensation for parasitic resistances of power traces would help achieve the goal of Furukawa of providing "a recording head with further miniaturization and good power efficiency." Ex. 1004 at 1:4-7, 7:49-51; Ex. 1006 at Abstract; *see also* Ex. 1007 ¶ 221.

2. Claim 2

Claim 2 requires "[t]he semiconductor substrate of claim 1, wherein the **fluid ejection actuators comprise heater resistors**," which is disclosed by Furukawa. Ex. 1007 ¶¶ 222-224.

As discussed in IX.B.1, limitation (A), incorporated herein, Furukawa uses **heaters 100**. *See, e.g.*, Ex. 1006 at [0023].

Therefore, Furukawa discloses "[t]he semiconductor substrate of claim 1, wherein the **fluid ejection actuators comprise heater resistors** [e.g., heaters 101]." Ex. 1007 ¶¶ 222-224.

3. Claim 3

Claim 3 requires "[t]he semiconductor substrate of claim 1, wherein the semiconductor substrate contains **at least three fluid supply slots** and associated ejection actuators, power transistors, logic circuits, and conductors," which Furukawa as modified by Torgerson discloses. Ex. 1007 ¶¶ 225-228.

As discussed in IX.B.1, limitation (A), incorporated herein, Furukawa as modified by Torgerson describes three ink feed slots (71). Ex. 1004 at Fig. 4A, 4:36-40.

A PHOSITA would have understood that each ink feed slot has its own columnar array of heater resistors, power transistors, logic circuits, and conductors. Ex. 1007 ¶ 227.

Therefore, Furukawa as modified by Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the semiconductor substrate contains **at least three fluid supply slots** [e.g., ink feed slots 71 of Torgerson] and associated

ejection actuators, power transistors, logic circuits, and conductors." Ex. 1007 ¶¶ 225-228.

4. Claim 4

Claim 4 requires "[t]he semiconductor substrate of claim 1, wherein the **power transistors comprise field effect transistors (FETS)**," which Furukawa as modified by Torgerson discloses. Ex. 1007 ¶¶ 229-232.

As discussed in Section IX.A.1, incorporated herein, a PHOSITA would have been motivated to modify the substrate of Furukawa to utilize Torgerson's FET drive circuits 85 as the power transistors wherein FET stands for field effect transistor.

Therefore, Furukawa as modified by Torgerson discloses "[t]he semiconductor substrate of claim 1, wherein the **power transistors comprise field effect transistors (FETS)** [e.g., Torgerson's FET drive circuits 85]." Ex. 1007 ¶¶ 229-232.

5. Claim 5

Claim 5 requires "[t]he semiconductor substrate of claim 1, wherein the **logic circuits** comprises [*sic*] circuits selected from the group consisting of **primitive address logic**, **predrive circuits,** data registers, and combinations of two or more of the foregoing," which Furukawa discloses. Ex. 1007 ¶¶ 233-235.

Furukawa explains that "103 is a drive logic circuit group comprising a shift register, a latch circuit, a switch, etc." Ex. 1006 at [0023]. A PHOSITA would have

understood that a shift register is used to address logic and is also known as a predrive circuit. Ex. 1007 ¶ 234.

Therefore, Furukawa discloses "[t]he semiconductor substrate of claim 1, wherein the logic circuits comprises [*sic*] circuits selected from the group consisting of **primitive address logic**, **predrive circuits,** data registers, and combinations of two or more of the foregoing." Ex. 1007 ¶¶ 233-235.

6. Claim 8

Claim 8 requires "[a] **micro-fluid ejection head** comprising the substrate of claim 1," which Torgerson discloses. Ex. 1007 ¶¶ 236-239.

As discussed in Section IX.A.6, incorporated herein, the term "micro-fluid ejection head" in the '341 Patent is used interchangeably with the term "micro-fluid ejection device" and would have been understood to be synonymous with the term ink jet recording head. *See also* Ex. 1007 ¶ 237. As discussed in Section IX.B.1, preamble, incorporated herein, Furukawa discloses the board in Figures 3-4 being part of recording head IJH. Ex. 1006 at [0001, 0016, 0021].

Therefore, Furukawa discloses "[a] **micro-fluid ejection head** [e.g., recording head IJH] comprising the substrate of claim 1 [Figs. 3-4]." Ex. 1007 ¶¶ 236-239.

X. SECONDARY CONSIDERATIONS

As it is the Patent Owner's burden to assert secondary considerations, to the extent that Patent Owner raises any such arguments in its Preliminary Response, Petitioners request authorization to respond thereto before any Institution Decision.

XI. CONCLUSION

Trial should be instituted, and the Challenged Claims should be cancelled as unpatentable.

Dated: August 23, 2022

Respectfully Submitted,

/ *Dion M. Bregman* /
Dion M. Bregman (Reg. No. 45,645)

U.S. PATENT NO. 7,195,341 – Claim Listing

No.	Claim Elements
Claim 1[P]	A semiconductor substrate for a micro-fluid ejection device, the substrate comprising:
1[A]	a plurality of micro-fluid ejection actuators disposed in a columnar array adjacent a fluid supply slot in the semiconductor substrate;
1[B]	a plurality of power transistors disposed in a columnar array adjacent the ejection actuators and connected through a first metal conductor layer to the ejection actuators, the columnar array of power transistors occupying a power transistor active area of the substrate;
1[C]	a columnar array of logic circuits disposed adjacent the columnar array of power transistors and connected through a polysilicon conductor layer to the power transistors, the columnar array of logic circuits occupying a logic circuit area of the substrate;
1[D]	a power conductor for the ejection actuators routed in a second metal conductor layer disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate; and
1[E]	a ground conductor for the ejection actuators routed in the second metal conductor layer disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate.
Claim 2	The semiconductor substrate of claim 1, wherein the fluid ejection actuators comprise heater resistors.
Claim 3	The semiconductor substrate of claim 1, wherein the semiconductor substrate contains at least three fluid supply slots and associated ejection actuators, power transistors, logic circuits and conductors.
Claim 4	The semiconductor substrate of claim 1, wherein the power transistors comprise field effect transistors (FETS).
Claim 5	The semiconductor substrate of claim 1, wherein the logic circuits comprises circuits selected from the group consisting of primitive address logic, predrive circuits, data registers, and combinations of two or more of the foregoing.
Claim 8	A micro-fluid ejection head comprising the substrate of claim 1.

CERTIFICATION OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Petition includes 13,665 words as counted by Microsoft Word and is therefore in compliance with the 14,000-word limit established by 37 C.F.R. 42.24(a)(1)(i). Accordingly, pursuant to 37 C.F.R. 42.24(d), lead counsel for the Petitioners hereby certify that this petition complies with the type-volume limits established for a petition requesting IPR.

Dated: August 23, 2022

Respectfully Submitted,

/ *Dion M. Bregman* /
Dion M. Bregman (Reg. No. 45,645)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. 42.6(4) and 42.105, lead counsel for Petitioners hereby certify that on August 23, 2022, copies of this Petition and all supporting exhibits were sent via Priority Mail Express to the correspondence address of record for the '341 patent:

133676 - Goldberg Segalla LLP
711 3rd Avenue, Suite 1900
New York, NY 10017

A courtesy copy of this Petition and supporting exhibits was also served via email on August 23, 2022 on Patent Owner's counsel of record in the district court litigation against Slingshot Printing LLC involving this patent:

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Dated: August 23, 2022

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