UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Canon U.S.A., Inc., and Canon Inc.,

Petitioners

v.

Slingshot Printing LLC,

Patent Owner

Case No. IPR2022-01415

Patent No. 7,559,629

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,559,629 (CLAIMS 1-10 and 13-14)

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 311 and 37 C.F.R. § 42.100 et seq., Petitioners request *Inter Partes* Review ("IPR") of claims 1-10 and 13-14 (the "Challenged Claims") of U.S. Patent No. 7,559,629 ("the '629 Patent," Ex. 1001), purportedly owned by Slingshot Printing LLC ("Patent Owner").

II. MANDATORY NOTICES

Real Party-in-Interest: The real parties-in-interest are **Canon U.S.A., Inc.** and **Canon Inc.**

Related Matters: The '629 Patent has been asserted against Petitioner Canon U.S.A., Inc. as well as Canon Solutions America, Inc. in *Slingshot Printing LLC v. Canon U.S.A., Inc., et al.*, No. 2:22-cv-00123 (E.D.N.Y.), which was filed on January 7, 2022. The '629 Patent was also asserted against HP Inc. in *Slingshot Printing LLC v. HP Inc.*, No. 6:19-cv-00549, reassigned as No. 2:20-00187 (W.D. Tex.). That case was dismissed with prejudice on April 1, 2021 following the parties' joint stipulation of dismissal. To the best of Petitioners' knowledge, the '629 Patent has not been asserted against other parties.

Lead Counsel: Dion M. Bregman (Reg. No. 45,645); Back-up Counsel: Amanda S. Williamson (Reg. No. 73,683) and Jason E. Gettleman (Reg. No. 55,202).

Service: Service of any documents may be made on Morgan, Lewis & Bockius LLP, 1400 Page Mill Road, Palo Alto, CA, 94304 (Telephone: 650.843.4000; Fax: 650.843.4001). Petitioners consent to e-mail service at: CanonSlingshotIPRs@morganlewis.com.

III. IDENTIFICATION OF CLAIMS AND GROUNDS

'629 Patent: This patent was filed on September 29, 2005 and has an earliest possible priority date of **September 29, 2005**. It is subject to the pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

Hayasaki: U.S. Patent Publication No. 2004/0201639 titled "Printhead Substrate, Printhead and Printing Apparatus" to Kimiyuki Hayasaki ("Hayasaki," Ex. 1004), was **filed March 29, 2004** and published **October 14, 2004**, and is prior art under § 102(a) and § 102(e).

Silverbrook: U.S. Patent Publication No. 2003/0020784 titled "Power Distribution for Inkjet Printheads" to Kia Silverbrook ("Silverbrook," Ex. 1005), was filed on April 16, 2001 and published **January 30, 2003**, and is prior art under § 102(b).

Krouss: U.S. Patent No. 6,190,000 titled "Method and Apparatus for Masking Address Out Failures" to Paul R. Krouss and Joseph M. Torgerson ("Krouss," Ex. 1012), was filed on August 30, 1999 and published **February 20, 2001**, and is prior art under § 102(b).

Petitioners request that the Board find each of the Challenged Claims invalid on the following grounds:

Ground	Prior Art	Statutory Basis	Claims
1	Hayasaki	§ 102	1-10 and 13-14
2	Hayasaki and Silverbrook	§ 103	1-10 and 13-14
3	Hayasaki and Krouss	§ 103	1-10 and 13-14

IV. CERTIFICATION AND FEES

Petitioners certify that the '629 Patent is available for IPR and that Petitioners are not barred or estopped from requesting this IPR on the grounds identified herein.

Any additional fees may be charged to Deposit Account No. 50,0310 (Order No. 132261-0003).

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

The PTAB should not exercise its discretion to deny review where, as here, the Petition is particularly strong in the underlying merits. *See, e.g.*, *Apple Inc. v. RFCyber Corp*., IPR2022-00412, Paper 11 at 33-34 (PTAB July 21, 2022); Interim Procedure for Discretionary Denials In AIA Post Grant Proceedings With Parallel District Court Litigation, PTO Director's Memorandum, p.9 (June 21, 2022).

Moreover, the stage of the parallel district court litigation does not support denying institution based on the *Fintiv* factors.

Factor 1 is neutral because no party has (yet) requested a stay.

Factor 2 favors institution because the district court litigation is in its early stage with **no trial date yet set**. The last set date in the parties' Case Management Schedule is Reply *Daubert* motions set for October 25, 2024, meaning trial cannot occur until **after October 25, 2024**. Ex. 1009 at 6. Moreover, the median time to trial in the Eastern District of New York is 48.9 months (~4 years). Thus, the final written decision will be issued well before any trial date that may occur under the parties' current Case Management Schedule or under the median time to trial in the Eastern District of New York.

Factor 3 favors institution because the district court litigation is in its early stages with invalidity contentions not due until October 17, 2022, and the parties exchanging claim construction terms on April 7, 2023. Ex. 1009 at 4. Thus, by the time of the institution deadline, the Court would not have issued any claim construction rulings and likely would not have ruled on any dispositive motions nor considered any invalidity issues based on the prior art.

Factor 4 favors institution because Petitioners challenge multiple claims (claims 4-7, 9-10, and 14) that have not been asserted in the district court litigation. Ex. 1011 ¶ 62 (asserting claims 1-3, 8, and 13). The invalidity contentions will include prior art cited in this Petition making it more efficient for the Board to handle the overlapping prior art.

Factor 5 is neutral because Petitioner Canon U.S.A., Inc. is a defendant in the district court litigation, but Petitioner Canon Inc. is not a party to that litigation.[1]

Factor 6 favors institution and is **dispositive** under the Guidance because the **unpatentability challenges here are compelling** and **rely on references that were not before the Office**. Additionally, this IPR is the only challenge to the '629 Patent that has been before the Board, which favors institution, and a strong public interest against "leaving bad patents enforceable" exists. *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

Because all *Fintiv* factors favor institution or are neutral, Petitioners respectfully request the Board decline to discretionarily deny review.

VI. BACKGROUND

A. The '629 Patent

The '629 Patent describes an inkjet printhead and "apparatuses for implementing multi-via heater chips." Ex. 1001 at Abstract, 1:7-9. The '629 Patent notes "the traditional use of [a] single heater array on a single side of an ink via limits the achievable printing resolution, including the vertical resolution." Ex. 1001 at 1:23-25. It also notes that "connections between the logic arrays and the heater

[1] Note that Canon Solutions America, Inc. in the parallel district court litigation is not a real-party-in interest in this proceeding.

arrays they address occupy a significant amount of space on the heater chips." Ex. 1001 at 1:30-32. As such, the '629 Patent explains "there is a need in the industry for heater chips that can provide for enhanced printing resolutions while reducing chip die sizes." Ex. 1001 at 1:42-44.

Figure 2 of the '629 Patent "illustrates ink vias disposed between heater arrays" according to an embodiment of the invention. Ex. 1001 at 3:32-34.

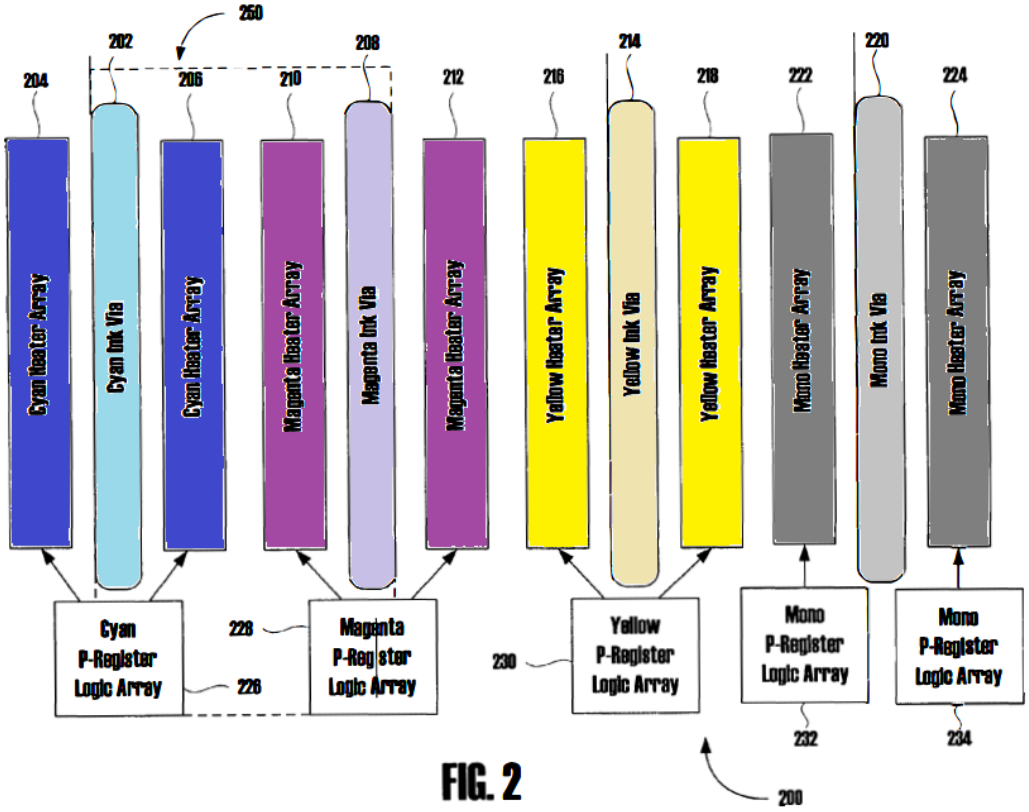


FIG. 2

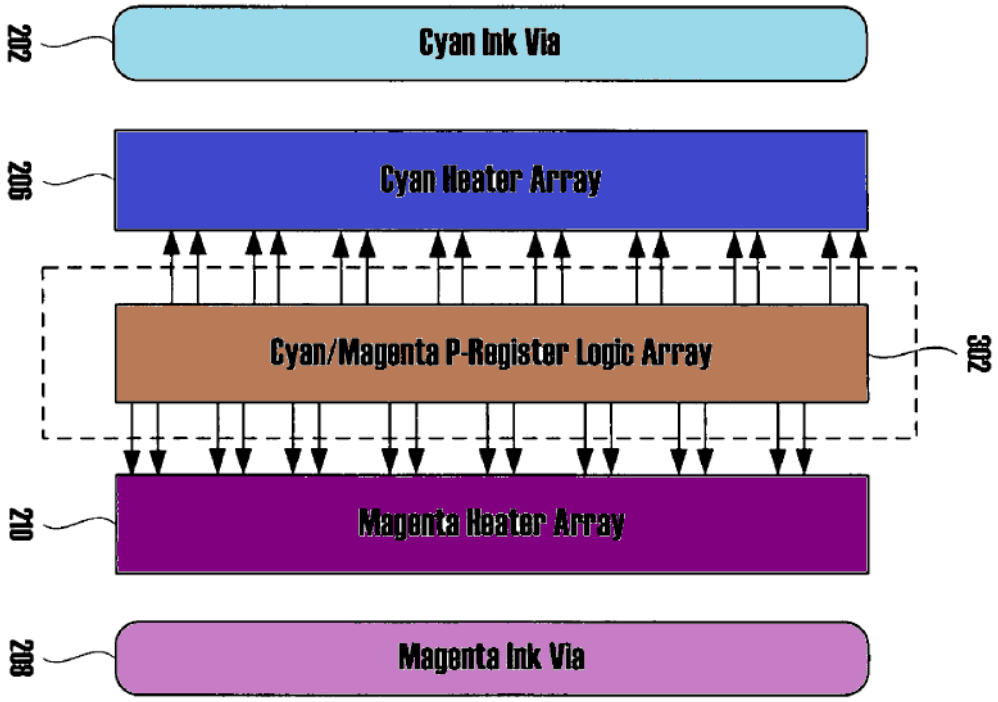
Ex. 1001 at Fig. 2.[2]

[2] All annotations in figures added unless otherwise noted.

In Figure 2, the "heater chip 200 includes four ink vias [cyan ink via 202, light blue; magenta ink via 208, light purple; yellow ink via 214, light yellow; monochrome ink via 220, light gray] each disposed between two heater arrays [204, 206, dark blue; 210, 212, dark purple; 216, 218, dark yellow; 222, 224, dark gray, respectively]." Ex. 1001 at 4:16-26. Each of the heater arrays may be "addressed and controlled, at least in part, by logic arrays." Ex. 1001 at 4:56-60.

Figure 3 "illustrates an exemplary configuration for a **single hybrid, non-contiguous** P-register logic array between two heater arrays." Ex. 1001 at 3:35-38.[3] A portion of the cyan P-register logic array 226 is **"interleave[d]"** with a portion of the magenta P-register logic array 228 "to form a **single hybrid** cyan/magenta P-register logic array 302 [brown] positioned between the second cyan heater array 206 [dark blue] and the first magenta heater array 210 [dark purple]." Ex. 1001 at 5:43-53.

[3] Emphasis added unless otherwise noted.



Ex. 1001 at Fig. 3.

B. The Prosecution History of the '629 Patent

The application leading to the '629 Patent was filed on September 29, 2005. Ex. 1003 at 14-17. After a Restriction Requirement, Applicant cancelled original claims 15-20. Ex. 1003 at 36, 40; Ex. 1007 ¶ 38.

The Patent Office made multiple prior art rejections, and Applicant amended its original claims multiple times. Ex. 1007 ¶¶ 39-42; Ex. 1003 at 52-59, 68-69, 76-84, 90-91, 134-142, 178-179, 199-207, 248-249. Upon allowance, no explanation was provided. Ex. 1003 at 254-259; Ex. 1007 ¶ 43.

None of the references cited herein were considered by the Patent Office during prosecution of the '629 Patent.

C. The Prior Art

1. Hayasaki (Ex. 1004)

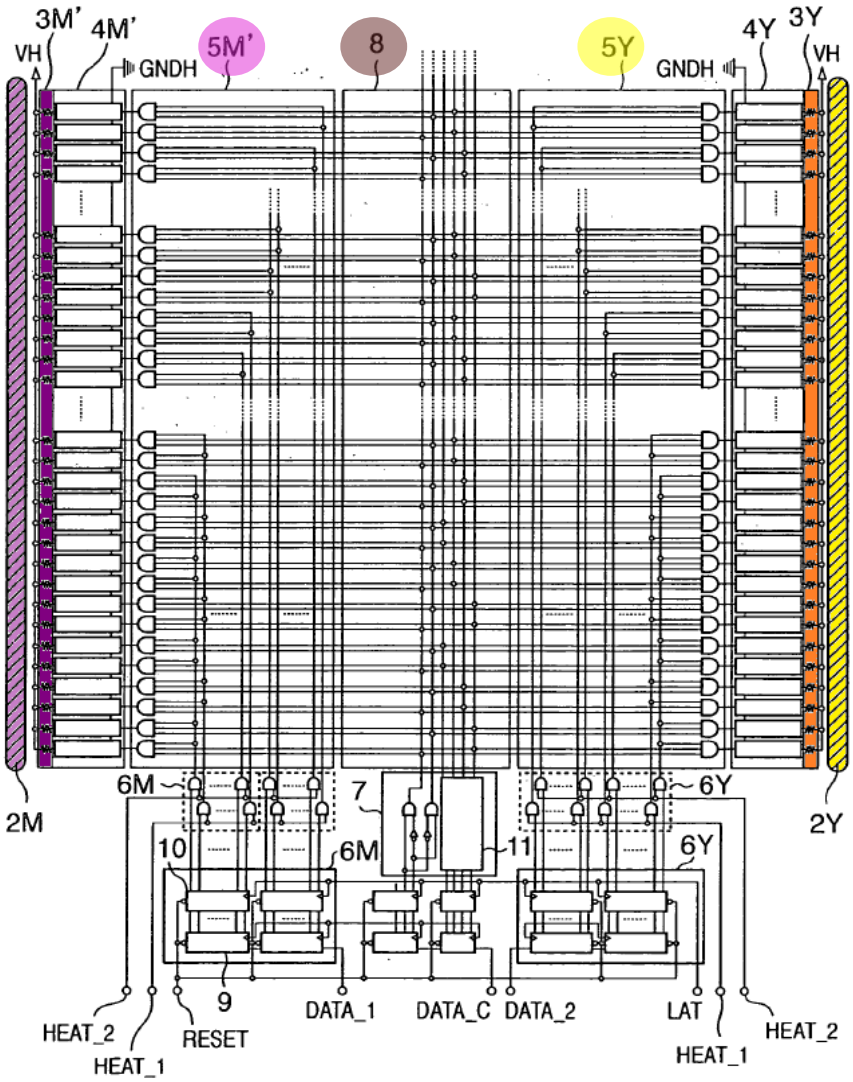
Hayasaki describes "a printhead substrate capable of controlling the driving of a large number of printing elements **in a reduced surface area**." Ex. 1004 at Abstract.

Like the '629 Patent, Hayasaki describes a drawback of prior art systems utilizing a multi-channel printhead is they require more complicated configurations that **drive up the cost and size of the printhead**. Ex. 1004 at [0013-0022]. Like the '629 Patent, Hayasaki seeks to address these problems by providing a printhead substrate that "is capable of controlling the driving of a larger number of printing elements in a **reduced surface area**." Ex. 1004 at [0024].

To achieve the reduced substrate size, Hayasaki discloses the same claimed layout as in the '629 Patent: an **inkjet printhead chip (IJHC)** comprising a **first heater array (3M', dark purple)**; a **first ink via (2M, light purple)** on the left side of the **first heater array (3M', dark purple)**; a **second heater array (3Y, orange)** wherein the right side of the **first heater array (3M', dark purple)** faces the left side of the **second heater array (3Y, orange)**; a **second ink via (2Y, yellow)** on the right side of the **second heater array (3Y, orange);** and a **logic array (AND circuit array 5M' (purple circle), wiring 8 (brown circle), AND circuit array 5Y (yellow**

circle)) disposed substantially between the **first heater array (3M', dark purple)** and the **second heater array (3Y, orange)**. Ex. 1004 at Fig. 9, [0057-0062, 0093].

FIG. 9



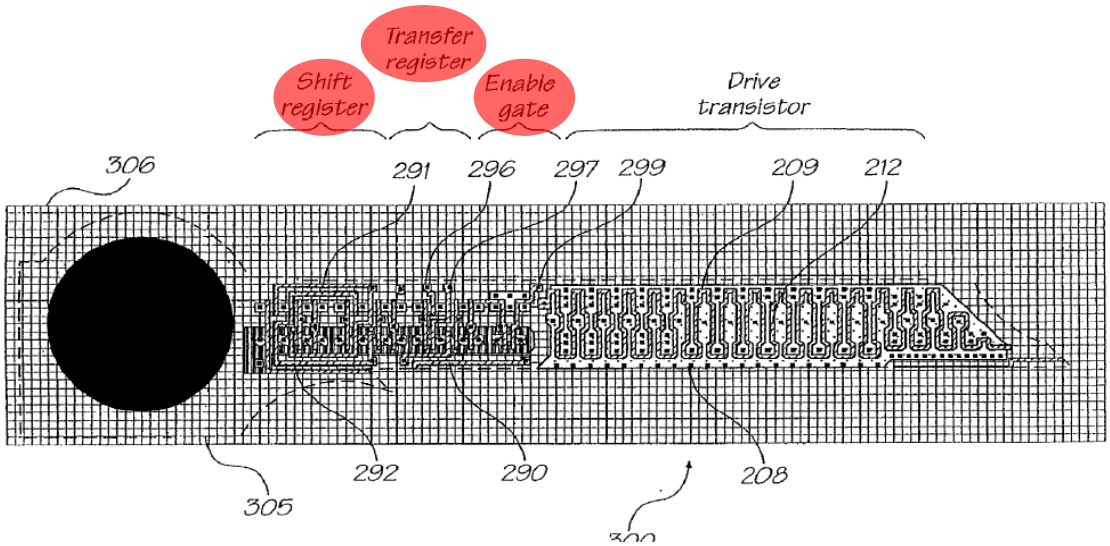
Ex. 1004 at Fig. 9.

2. Silverbrook (Ex. 1005)

Silverbrook is directed to "[a]n inkjet printhead" that includes control logic 280 "utilized to activate a heater element 281 on demand." Ex. 1005 at Abstract,

[0300]. "The **control logic 280 includes a shift register 282, a transfer register 283 and a firing control gate 284**." Ex. 1005 at [0300-0301].

Figure 79 depicts "the general layout" including the shift register (red), transfer register (red) and enable gate (red) of a unit cell 305. Ex. 1005 at [0305].



Ex. 1005 at Fig. 79.

Figure 86 shows an enlarged view of the array of ink ejection nozzles depicted in Figure 85 wherein the logic cells associated with one array of ink ejection nozzles (pink) are interleaved with the logic cells associated with the other array (blue). Ex. 1005 at [0194-0195, 0311].

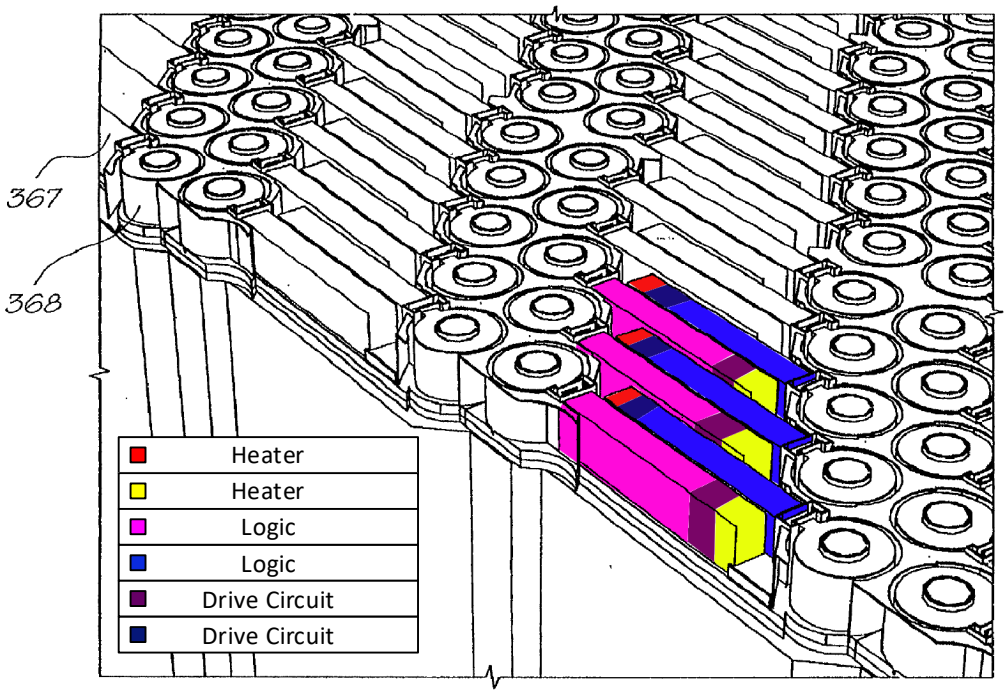


FIG. 86

Ex. 1005 at Fig. 86.

3. Krouss (Ex. 1012)

Krouss teaches "an inkjet printhead for use in an inkjet printing system for depositing ink on media." Ex. 1012 at Abstract. Figure 5 depicts a "bottom plan view of the inkjet printhead 24" including drop generators 30, 32, and 34 for depositing yellow, magenta, and cyan inks, respectively. Ex. 1012 at Fig. 5, 6:54-57.

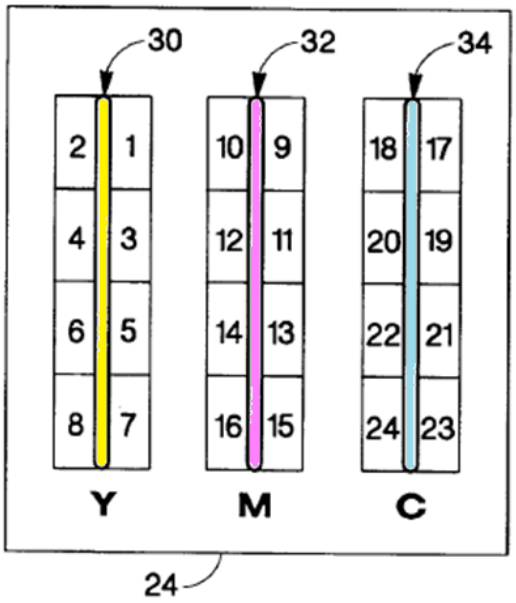


Fig. 5

Ex. 1012 at Fig. 5.

Krouss explains "the drop generators are arranged in parallel rows adjacent the ink feed slot 48" with the nozzles associated with the yellow ink (and similarly magenta and cyan ink] drop generators **offset along a longitudinal axis** of the slot 48. Ex. 1012 at 7:18-26, 7:51-57.

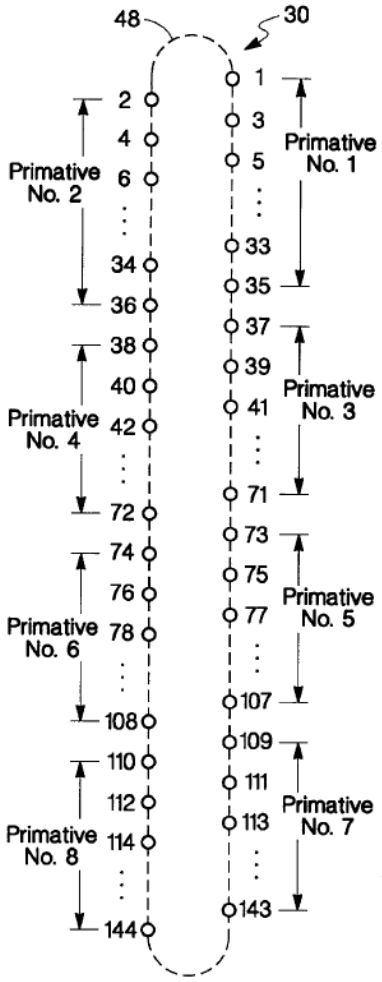


Fig. 6

Ex. 1012 at Fig. 6.

VII. LEVEL OF SKILL

A person having ordinary skill in the art ("POSITA") at the time of the alleged invention would have been a person holding at least a Bachelor's level college degree in Mechanical Engineering, Electrical Engineering, Physics, Computer

Science or a related field, and at least two years of training or experience in the design of inkjet printheads. Ex. 1007 ¶ 45.

VIII. CLAIM CONSTRUCTION

In *Slingshot Printing LLC v. HP Inc.*, Judge Albright construed the following terms, which Petitioners propose here. *See, e.g.*, Ex. 1010 at 3-4; Ex. 1007 ¶¶ 46-49.

Term	Construction from Judge Albright
"non-contiguous hybrid arrangement" (claims 1, 8)	"[a]n arrangement in which the first set of logic cells are interleaved or interlaced with the second set of logic cells" Ex. 1010 at 4.
"ink via" (claims 1-4, 8, 9, 14)	"[a] path to fluidly connect the supply of ink to one or more heaters" Ex. 1010 at 4.
"at least one logic array" (claims 1, 4, 5)	"at least one group of logic cells" Ex. 1010 at 3.
"a first logic array" (claims 4 and 8)	"a first group of logic cells" Ex. 1010 at 3.

"allows the first ink via and second ink via to be simultaneously controlled by" (claims 1, 8)	"Plain and ordinary meaning" Ex. 1010 at 3.
"substantially between the first heater array and the second heater array" (claims 1, 8)	"Plain and ordinary meaning" Ex. 1010 at 3.

As "a first logic array" was construed to mean "a first group of logic cells," the term "a second logic array" appearing in claim 4 should similarly be construed to mean "a second group of logic cells" because this construction is consistent with that adopted by Judge Albright with respect to the term "first logic array." Ex. 1007 ¶ 49.

Petitioners propose that the remaining claim terms in the Challenged Claims be afforded their plain and ordinary meaning.

IX. ARGUMENT

A. Ground #1: Claims 1-10 and 13-14 are anticipated by Hayasaki

1. Claim 1[4]

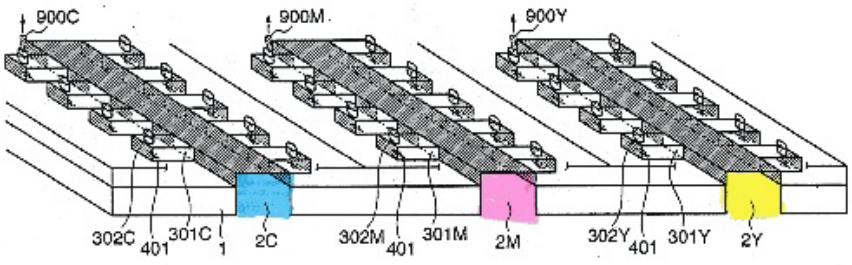
a. 1[P]: "A chip for use in a printing device"

Generally, the preamble is not limiting. To the extent the preamble is a limitation of the claim, Hayasaki discloses this limitation. Ex. 1007 ¶¶ 83-87.

Specifically, the **tri-color inkjet printhead IJHC** of Hayasaki corresponds to the claimed chip for use in a printing device. Ex. 1007 ¶¶ 83-87.

Figure 3 "is a perspective view showing a three-dimensional structure of a printhead IJHC that discharges three colors of ink." Ex. 1004 at [0057].

FIG. 3



Ex. 1004 at Fig. 3.

In Figure 3, "reference numeral 1 denotes a printhead substrate (hereinafter **referred to as a "head substrate"**) on which are formed electrothermal transducers and the variety of circuits that drive the electrothermal transducers to be described

[4] A full claim listing can be found in the Appendix.

later, a memory, a variety of pads that form the electrical contacts with the carriage HC, and a variety of signal wires." Ex. 1004 at [0060]. Ink channels 2C (cyan), 2M (magenta), and 2Y (yellow) are placed on the printhead. Ex. 1004 at Fig. 3, [0058].

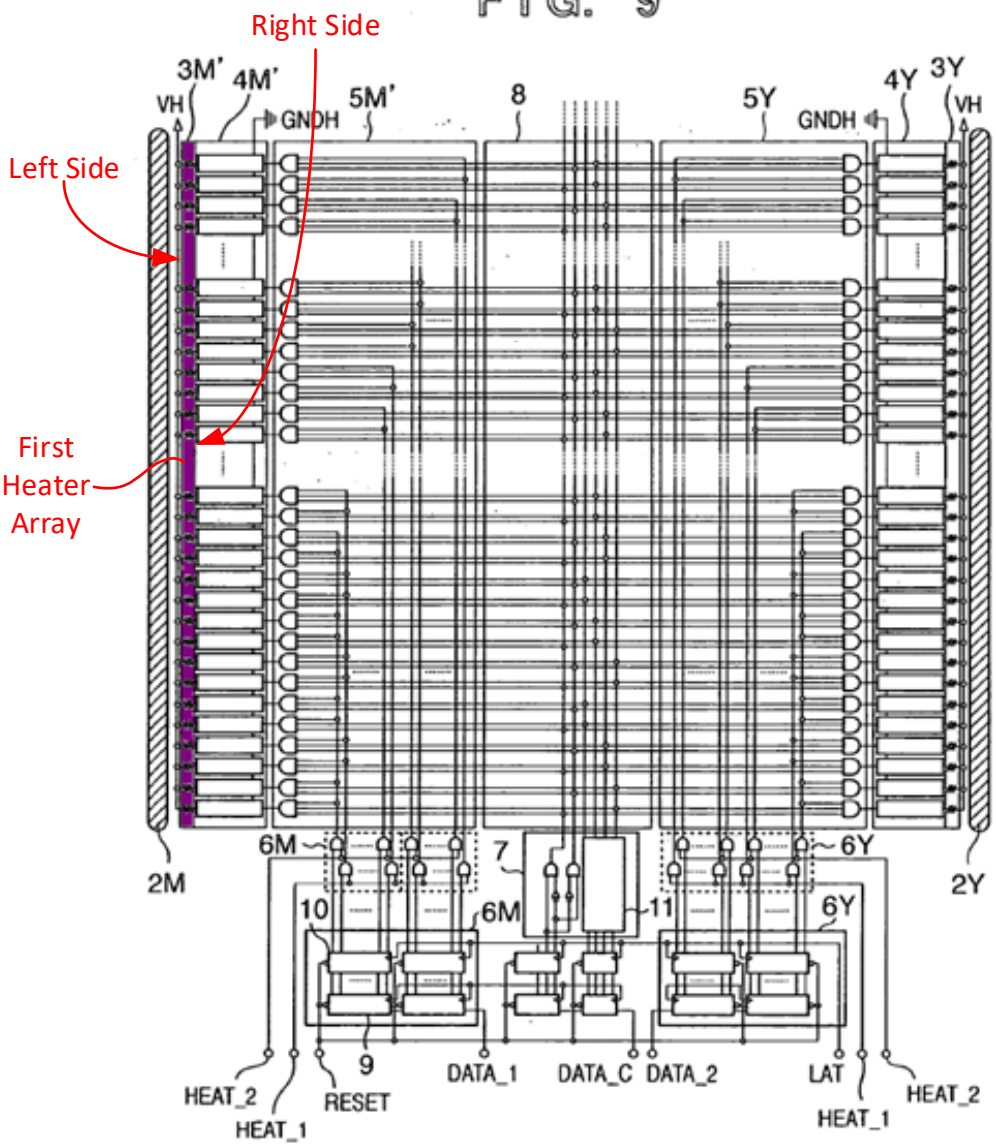
Therefore, Hayasaki discloses a "**chip** [e.g., printhead chip IJHC] for use in a printing device." Ex. 1007 ¶¶ 83-87.

b. 1[A]: "a first heater array with a left side and a right side"

Hayasaki discloses this limitation. Ex. 1007 ¶¶ 88-92.

Specifically, **printing element array 3M' (purple)** corresponds to the first heater array, and, as seen in Figure 9, it has a left side and a right side. Ex. 1007 ¶ 89.

FIG. 9



Ex. 1004 at Fig. 9.

Hayasaki explains "a printing element array ha[s] a **plurality of printing elements**," and "one electrothermal transducer (heater), the MOS-FET that drives it and the **electrothermal transducer (heater) are together called a printing**

element, with a plurality of printing elements called a printing element." Ex. 1004 at [0025, 0061].

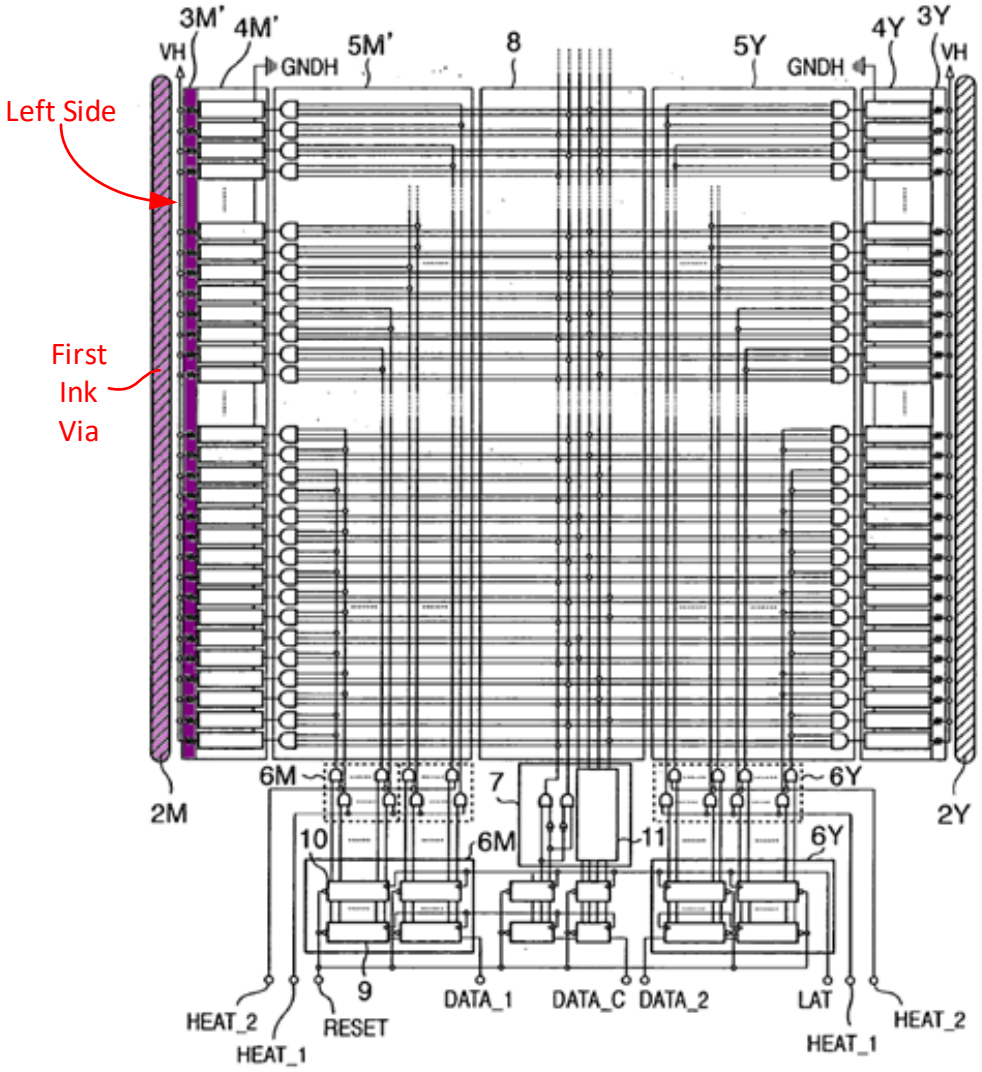
As such, the printing element array 3M' in Hayasaki corresponds to the claimed first heater array because a printing element array has a plurality of printing elements with each printing element including an electrothermal transducer (heater). Ex. 1007 ¶ 90. Indeed, Hayasaki further notes that in Figure 9, "[t]he ink channels 2M and 2Y are respectively connected to the **printing element arrays 3M'** and 3Y," and "an **electric current that causes ink discharge** is sent through the relevant **printing elements of the printing element arrays 3M'** and 3Y." Ex. 1004 at [0093].

Therefore, Hayasaki discloses "a **first heater array** [e.g., printing element array 3M'] with a **left side** [e.g., Fig. 9] and a **right side** [e.g., Fig. 9]." Ex. 1007 ¶¶ 88-92.

c. 1[B]: "a first ink via placed on the left side of the first heater array"

Hayasaki discloses this limitation. Ex. 1007 ¶¶ 93-96. In Hayasaki, **ink channel 2M (light purple)** corresponds to the first ink via, and as seen in Figure 9, it is placed on the left side of the **first heater array (printing element array 3M', dark purple)**. Ex. 1007 ¶ 94.

FIG. 9



Ex. 1004 at Fig. 9.

As discussed in Section VIII, the term "ink via" should be construed to mean "[a] path to fluidly connect the supply of ink to one or more heaters." *See* Section VIII.

Hayasaki explains that in Figure 9, "[t]he **ink channels 2M** and 2Y are respectively connected to the printing element arrays 3M' and 3Y." Ex. 1004 at

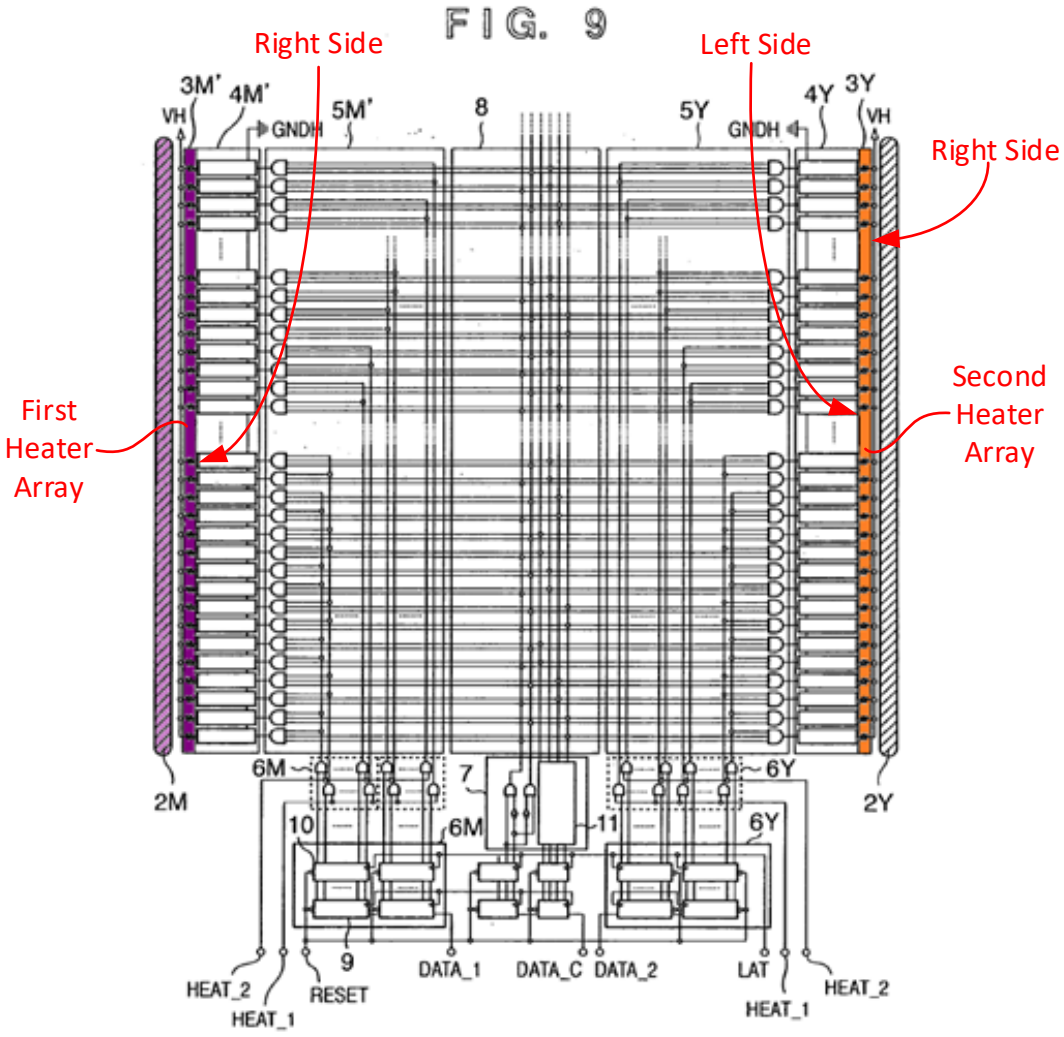
[0093]. It further notes that "**ink channel 2M** that supplies magenta (M) ink." Ex. 1004 at [0058]. Ink channel 2M thus corresponds to the claimed ink via as that term is understood. Ex. 1007 ¶ 95.

Therefore, Hayasaki discloses "a **first ink via** [e.g., ink channel 2M] placed on the **left side** [e.g., Fig. 9] of the **first heater array** [e.g., printing element array 3M']." Ex. 1007 ¶¶ 93-96.

d. 1[C]: "a second heater array with a left side and a right side, wherein a right side of the first heater array faces the left side of the second heater array"

Hayasaki discloses this limitation. Ex. 1007 ¶¶ 97-101.

In Hayasaki, **printing element 3Y (orange)** corresponds to the claimed second heater array, and, as seen in Figure 9, it has a left side and a right side with the right side of the first heater array (3M', dark purple) facing the left side of the second heater array (3Y, orange). Ex. 1004 at Fig. 9; Ex. 1007 ¶ 98.



Ex. 1004 at Fig. 9.

As discussed in Section IX.A.1.b, incorporated here, the printing element arrays described in Hayasaki correspond to the heater arrays. Thus, printing element array 3Y corresponds to the claimed second heater array. *See also* Ex. 1007 ¶¶ 99-100.

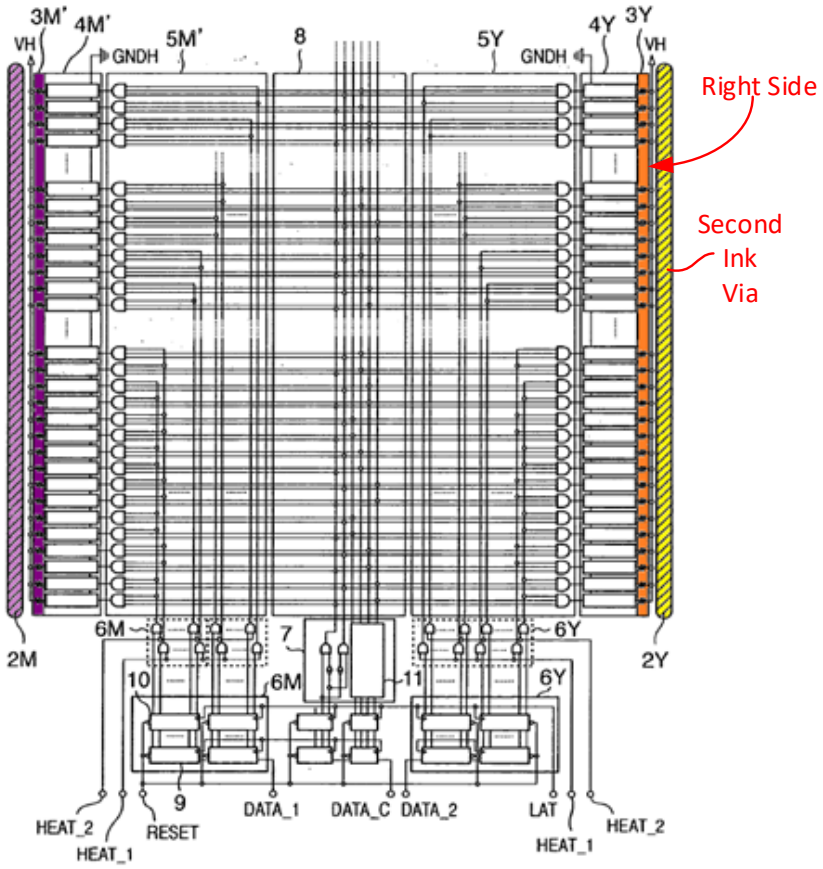
Therefore, Hayasaki discloses "a **second heater array** [e.g., printing element array 3Y] with a **left side** and a **right side** [e.g., Fig. 9], wherein a **right side** of the

first heater array [e.g., printing element array 3M'] **faces** [e.g., Fig. 9] the **left side** of the **second heater array** [e.g., 3Y]." Ex. 1007 ¶¶ 97-101.

e. 1[D]: "a second ink via placed on the right side of the second heater array"

Hayasaki discloses this limitation. Ex. 1007 ¶¶ 102-105. In Hayasaki **ink channel 2Y (yellow)** corresponds to the second ink via, and, as seen in Figure 9, it is placed on the right side of the **second heater array (printing element array 3Y, orange)**. Ex. 1004, Fig. 9; Ex. 1007 ¶ 103.

FIG. 9



Ex. 1004 at Fig. 9.

As discussed in Section VIII, the term "ink via" should be construed to mean "[a] path to fluidly connect the supply of ink to one or more heaters." *See* Section VIII.

In Figure 9, "[t]he **ink channels** 2M and **2Y** are respectively connected to the printing element arrays 3M' and 3Y." Ex. 1004 at [0093]. It further notes that "**ink channel 2Y** that supplies yellow (Y) ink." Ex. 1004 at [0058]. Ink channel 2Y thus corresponds to the claimed ink via as that term is understood. Ex. 1007 ¶ 104.

Therefore, Hayasaki discloses "a **second ink via** [e.g., ink channel 2Y] placed on the **right side** [e.g., Fig. 9] of the **second heater array** [e.g., printing element array 3Y]." Ex. 1007 ¶¶ 102-105.

f. 1[E]: "at least one logic array including a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement, the at least one logic array is disposed substantially between the first heater array and the second heater array wherein the first set of logic cells addresses and controls the first heater array and the second set of logic cells addresses and controls the second heater array, which allows the first ink via and second ink via to be simultaneously controlled by the at least one logic array"

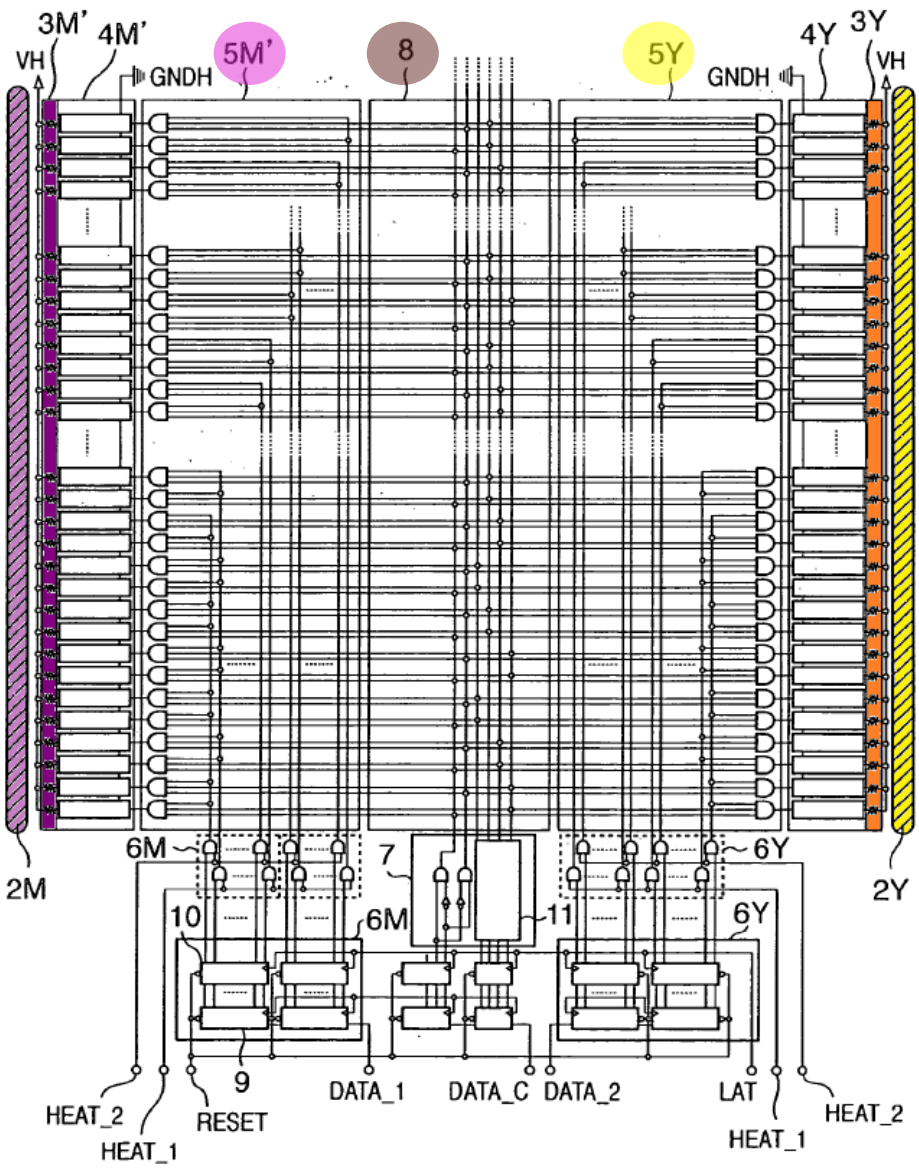
Hayasaki discloses this limitation. Ex. 1007 ¶¶ 106-126.

(i) 1[E], Part 1: "at least one logic array"

As seen in annotated Figure 9, Hayasaki discloses the claimed sets of logic cells that address and control the respective heater arrays, including **(i) the AND circuit array 5M' (purple circle) and its respective portion of the wiring 8**

(brown circle); and (ii) the AND circuit array 5Y (yellow circle) and its respective portion of the wiring 8 (brown circle). Ex. 1004 at Fig. 9, [0087, 0093, 0104-0106]; Ex. 1007 ¶ 107. This **combination of the AND circuit array 5M' (purple circle) and its respective portion of the wiring 8 (brown circle) and AND circuit array 5Y (yellow circle) and its respective portion of the wiring 8 (brown circle)** correspond to the claimed "at least one logic array." Ex. 1007 ¶¶ 107-113.

FIG. 9



Ex. 1004 at Fig. 9.

A POSITA would have understood that AND circuits are a type of logic cell depicted by the following symbol:

Ex. 1004 at Fig. 9; Ex. 1007 ¶ 108.

As seen in Figure 9, each of the AND circuit arrays 5M' and 5Y includes multiple AND logic cells arranged in a vertical column in parallel to its respective ink via (2M and 2Y) and driver array (4M' and 4Y). Ex. 1004 at Fig. 9; Ex. 1007 ¶ 108.

Hayasaki describes the AND circuit arrays 5M' and 5Y as **providing output logic** noting:

> The ink channels 2M and 2Y are respectively connected to the printing element arrays 3M' and 3Y, in turn, respectively connected to the driver arrays 4M' and 4Y, and in turn, respectively connected to **control wires and AND circuit arrays 5M' and 5Y that enable individual control of these elements. Depending on the output logic of each of the AND circuit arrays 5M' and 5Y**, the driver arrays 4M' and 4Y are driven individually so as to print. That is, an electric current that causes ink discharge is **sent through the relevant printing elements of the printing element arrays 3M' and 3Y**.

Ex. 1004 at [0093].

Hayasaki additionally explains:

> As shown in **FIG. 9**, in the case of a multi-channel printhead, two of the various circuit blocks descripted up to this point are disposed opposite each other between two of the ink channels. What can share these two circuit blocks for control is the circuit block and its associated wiring, which achieve time-division drive. **The most characteristic circuit block structure of the present embodiment is to arrange the shared wirings 8 for time-division drive between the above-described two circuit blocks. . . . In other words, the wiring 8 for time-division drive disposed at the center of the head substrate concurrently controls a plurality of printing elements** selectively by the control circuits 7 disposed on a place where the wiring 8 is extended.

Ex. 1004 at [0104-0106].

Thus, (i) the AND circuit array 5M' and its respective portion of wiring 8, and (ii) the AND circuit array 5Y and its respective portion of wiring 8, together correspond to the claimed "at least one logic array" because they all work together to provide output logic and address and control the plurality of printing elements. Ex. 1004 at [0093, 0104-0106]; Ex. 1007 ¶ 111. Figure 9 also illustrates a portion of the control of the printing elements emanating from the shared wiring located between AND circuit array 5M' and AND circuit array 5Y. Ex. 1004 at Fig. 9; Ex. 1007 ¶ 111.

Moreover, because the term "at least one logic array" should be construed to mean "at least one group of logic cells," (*see* Section VIII), the (i) AND circuit array 5M' and its respective portion of wiring 8, and (ii) the AND circuit array 5Y and its respective portion of wiring 8, together correspond to the claimed "at least one logic array" because each of the AND circuit arrays 5M'/5Y (and respective portion of wiring 8) includes multiple AND logic cells, i.e., at least one "group" of logic cells. Ex. 1007 ¶ 112.

(ii) 1[E], Part 2: "including a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement"[5]

The term "non-contiguous hybrid arrangement" means "[a]n arrangement in which the first set of logic cells are interleaved or interlaced with the second set of logic cells." *See* Section VIII.

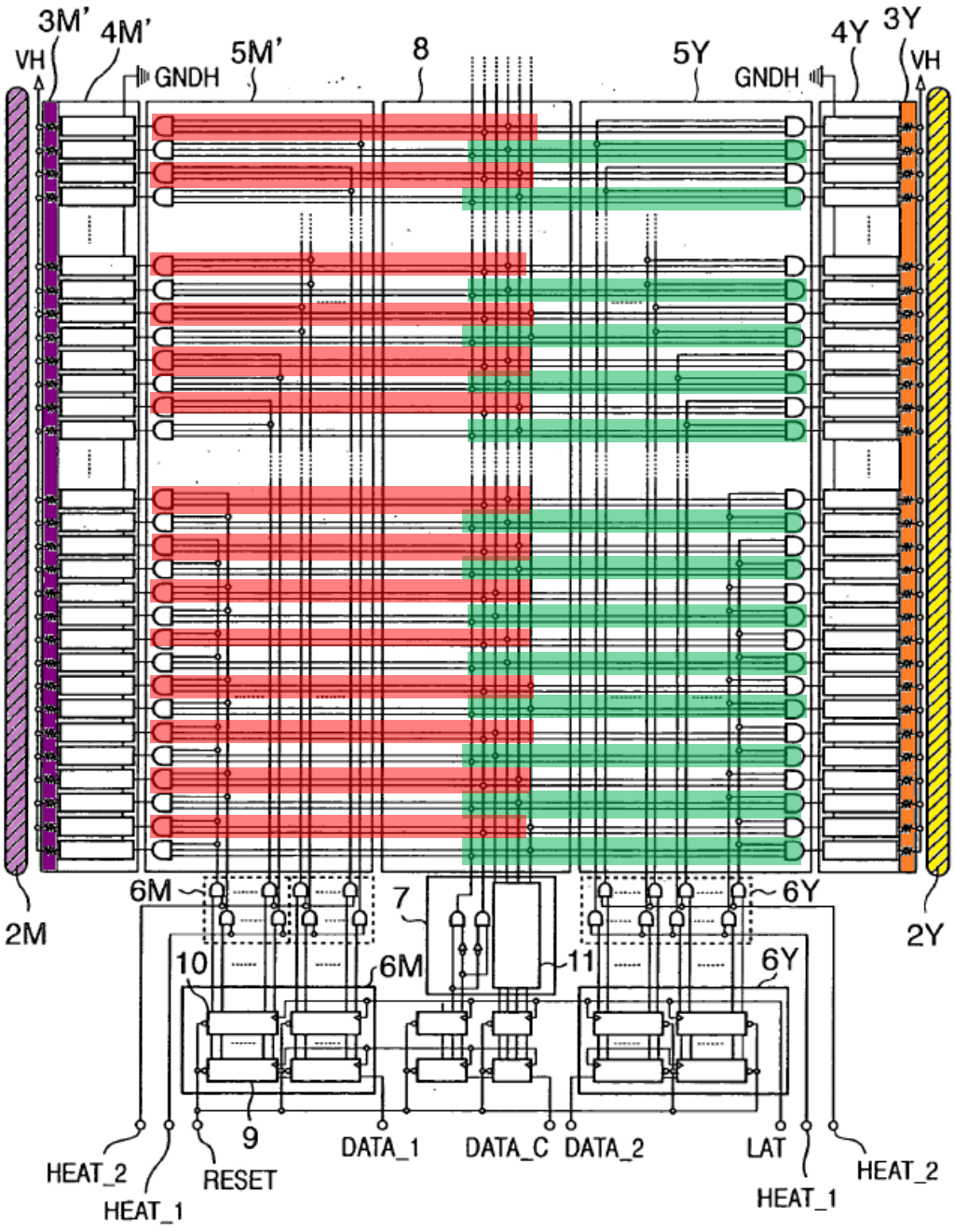
[5] As written, the limitation "a first and a second set of logic cells" is indefinite because it is unclear if this requires (i) a first set of logic cells and a second set of logic cells, (ii) first and second sets of logic cells, or (iii) a set of first logic cells and second logic cells. Because claim 1 also states "the first set of logic cells addresses and controls the first heater array," for purposes of this proceeding, Petitioners interpret this limitation as option (i) or (ii) to provide proper

Because the claim's preamble ends in the term "comprising," the claim is open-ended with the word "**comprising**" meaning "**including but not limited to**." *CIAS, Inc. v. All. Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007). Thus, although the claim requires the first set of logic cells are interleaved or interlaced with the second set of logic cells, **the claim is not restricted to a device that only has interleaved or interlaced logic cells**, i.e., the prior art may disclose other logic cells that are not relevant to the claims.

As seen in Figure 9, Hayasaki discloses numerous logic cells that are interleaved or interlaced with one another because it shows no less than fourteen pairs of interleaved logic cells, each including **a first set of logic cells (red boxes)** interleaved with a **second set of logic cells (green boxes)**. Ex. 1007 ¶¶ 115-116.

antecedent basis to "the first set of logic cells" limitation. Petitioners reserve all rights to raise indefiniteness arguments at a later stage.

FIG. 9



Ex. 1004 at Fig. 9.

In other words, as seen in annotated Figure 9 above, Hayasaki discloses a first set of logic cells (red boxes) and a second set of logic cells (green boxes) that are

arranged in a **non-contiguous hybrid arrangement** as that term is properly construed. *See* Section VIII; *see also* Ex. 1007 ¶¶ 117-122.

Hayasaki's disclosure of the first set of logic cells in red and the second set of logic cells in green interleaved with one another aligns with the plain language of the claim element that does not require **all** of the logic cells within the printhead be interleaved with one another. Therefore, the first set of logic cells shown in red above and the second set of logic cells shown in green above, which are interleaved with one another, meet the requirement of "a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement." Ex. 1007 ¶¶ 117-122.

Moreover, Hayasaki also operates its printing elements in an alternating or interleaved manner. Specifically, as Hayasaki explains, in **FIG. 9**, its circuits are configured **so as not to drive adjacent printing elements concurrently**" because "[i]f adjacent printing elements are to be driven concurrently, a phenomenon in which ink is insufficiently supplied adjacent nozzles (i.e., crosstalk) occurs because the inflow and outflow of ink occur at positions near each other." Ex. 1004 at [0095]. Therefore, in operation, no adjacent logic cells in each of the AND circuit arrays 5M' and 5Y are operational at the same time to avoid cross-talk phenomenon, which is consistent with the depiction of the claimed first set of logic cells (red boxes) and the second set of logic cells (green boxes). Ex. 1007 ¶¶ 120-122.

(iii) 1[E], Part 3: "the at least one logic array is disposed substantially between the first heater array and the second heater array"

As seen in Figure 9 above, the at least one logic array (AND circuit array 5M' (purple circle) and its respective portion of wiring 8 (brown circle) and the AND circuit array 5Y (yellow circle) and its respective portion of wiring 8 (brown circle)) is **disposed substantially between the first heater array (3M', purple) and the second heater array (3Y, orange).** Ex. 1004 at Fig. 9; Ex. 1007 ¶ 113.

(iv) 1[E], Part 4: "wherein the first set of logic cells addresses and controls the first heater array, and the second set of logic cells addresses and controls the second heater array, which allows the first ink via and second ink via to be simultaneously controlled by the at least one logic array"

Hayasaki explains:

> The ink channels 2M and 2Y are respectively connected to the printing element arrays 3M' and 3Y, in turn, respectively connected to the driver arrays 4M' and 4Y, and in turn, respectively connected to **control wires and AND circuit arrays 5M' and 5Y that enable individual control of these elements. Depending on the output logic of each of the AND circuit arrays 5M' and 5Y**, the driver arrays 4M' and 4Y are driven individually so as to print. That is, an electric current that causes ink discharge is **sent through the relevant printing elements of the printing element arrays 3M' and 3Y**.

Ex. 1004 at [0093].

Thus, the first set of logic cells (red boxes in Fig. 9 above) address and control the first heater array (3M') while the second set of logic cells (green boxes in Fig. 9 above) address and control the second heater array (3Y). Ex. 1007 ¶¶ 122-125. Hayasaki also explains:

> As shown in **FIG. 9**, in the case of a multi-channel printhead, two of the various circuit blocks descripted up to this point are disposed opposite each other between two of the ink channels. What can share these two circuit blocks for control is the circuit block and its associated wiring, which achieve time-division drive. **The most characteristic circuit block structure of the present embodiment is to arrange the shared wirings 8 for time-division drive between the above-described two circuit blocks. . . . In other words, the wiring 8 for time-division drive disposed at the center of the head substrate concurrently controls a plurality of printing elements** selectively by the control circuits 7 disposed on a place where the wiring 8 is extended.

Ex. 1004 at [0104-0106].

Hayasaki also explains that "the control wires are laid so as to provide **shared control over the plurality of printing element arrays** 3C and 3C', 3M and **3M'**, and **3Y** and 3Y', thus achieving a **head substrate area reduction**." Ex. 1004 at [0087].

Hayasaki also notes that "although two sets of input terminals (HEAT_1, HEAT_2) for control signals that control the pulse width of the print current to the printing elements as well as of the associated signal wires are provided for each of the two circuit blocks disposed opposite each other as described above, **it goes without saying that these terminals and signal wires may also be shared**." Ex. 1004 at [0109]; *see also* Ex. 1004 at [0111].

Thus, Hayasaki teaches that the first set of logic cells address and control their respective first heater array while the second set of logic cells address and control their respective second heater array, and the first ink via and second ink via can be simultaneously controlled by the at least one logic array. Ex. 1007 ¶¶ 122-125.

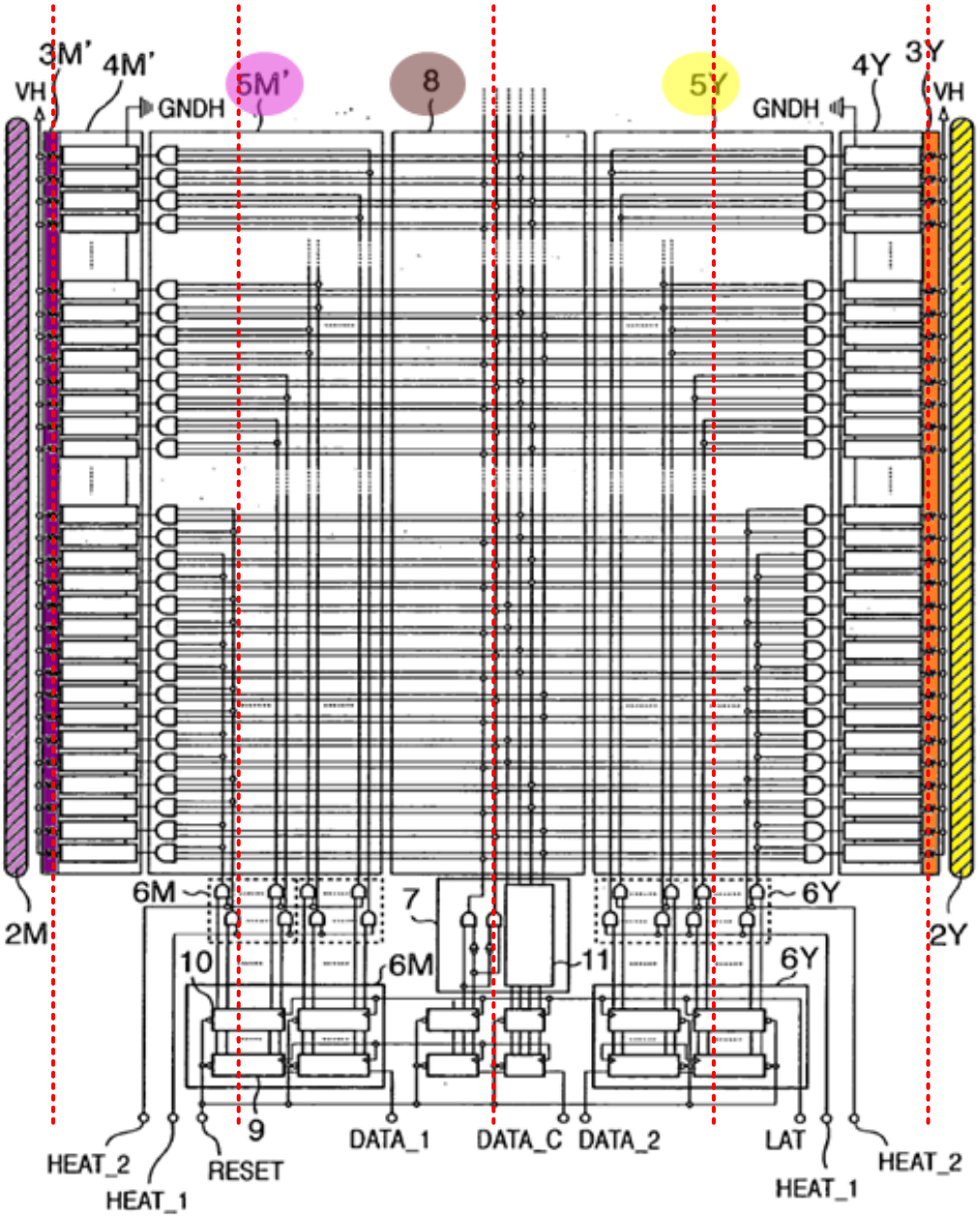
Accordingly, Hayasaki discloses "**at least one logic array** [e.g., AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8] including a **first** [e.g., red boxes in Fig. 9 above] and a **second set of logic cells** [e.g., green boxes in Fig. 9 above] arranged in a **non-contiguous hybrid arrangement** [e.g., interleaved as annotated Fig. 9 above], the at least one logic array is **disposed substantially between** [e.g., annotated Fig. 9 above] the **first heater array** [e.g., 3M'] and the **second heater array** [e.g., 3Y] wherein the first set of logic cells addresses and controls the first heater array and the second set of logic cells addresses and controls the second heater array, which

allows the **first ink via** [e.g., 2M] and **second ink via** [e.g., 2Y] to be simultaneously controlled by the at least one logic array." Ex. 1007 ¶¶ 106-126.

g. 1[F]: "wherein the at least one logic array is substantially parallel with the first heater array and second heater array"

As seen in Figure 9, the at least one logic array (AND circuit array 5M' (purple circle) and its respective portion of wiring 8 (brown circle) and AND circuit array 5Y (yellow circle) and its respective portion of wiring 8 (brown circle)) is **substantially parallel** with the first heater array (3M', purple) and second heater array (3Y, orange). Ex. 1007 ¶ 128. This can be seen below with the longitudinal axes for each of the AND circuit array 5M'(purple circle), the wiring 8 (brown circle), the AND circuit array 5Y (yellow circle), the first heater array (3M', purple), and the second heater array (3Y, orange), all being parallel to one another.

FIG. 9



Ex. 1004 at Fig. 9.

Therefore, Hayasaki discloses "wherein the **at least one logic array** [e.g., AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8] is substantially parallel with the **first**

heater array [e.g., 3M'] and **second heater array** [e.g., 3Y]." Ex. 1007 ¶¶ 127-130.

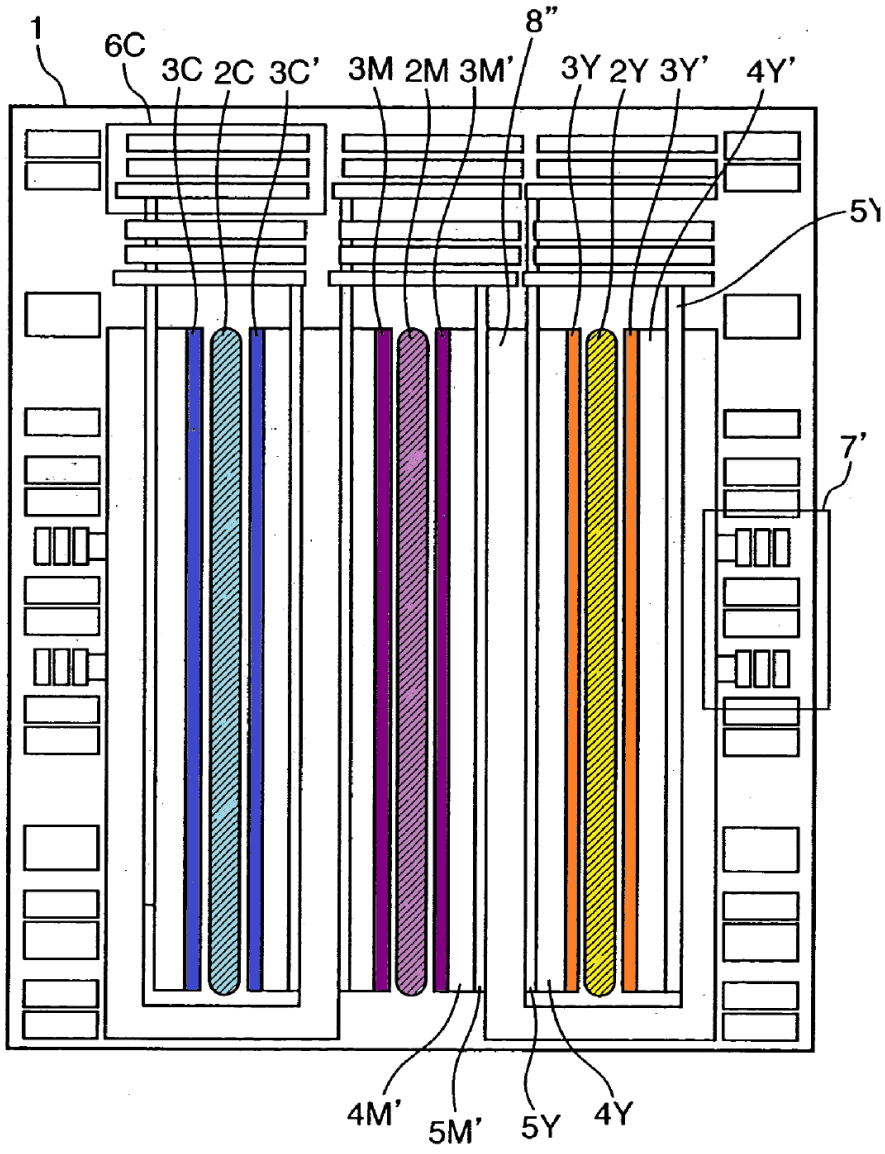
2. Claim 2

Claim 2 requires "[t]he chip of claim 1, further comprising a **third heater array** and a **fourth heater array**, wherein the **third heater array and first heater array sandwich the first ink via** and the **fourth heater array and the second heater array sandwich the second ink via**," which is disclosed by Hayasaki. Ex. 1007 ¶¶ 131-135.

In Hayasaki, **printing element array 3M** corresponds to the third heater array and **printing element array 3Y'** corresponds to the fourth heater array. Ex. 1007 ¶¶ 131-135.

As seen in Figure 7, the **third heater array (3M, purple) and first heater array (3M', purple)** sandwich (or bracket) the **first ink via (2M, light purple)**, and the **fourth heater array (3Y', orange)** and the **second heater array (3Y, orange)** sandwich (or bracket) the **second ink via (2Y, yellow)**. Ex. 1004 at [0085], Fig. 7; Ex. 1007 ¶ 133.

FIG. 7



Ex. 1004 at Fig. 7.

Although in the discussion of claim 1 above, reference was made to Figure 9, as Hayasaki explains, Figure 9 "is an equivalent circuit diagram showing the drive control configuration of a head substrate **having the layout shown in FIGS. 7-8**."

Ex. 1004 at [0092]. Hayasaki further explains that "[i]t should be noted that although the embodiment described above [in Fig. 9] refers only to the configuration between the ink channel that supplies magenta ink and the ink channel that supplies yellow ink, it goes without saying that **the same layout can be implemented between the ink channel that supplies cyan ink and the ink channel that supplies magenta ink**." Ex. 1004 at [0112].

Therefore, Hayasaki discloses "[t]he chip of claim 1, further comprising a **third heater array** [e.g., 3M] and a **fourth heater array** [e.g., 3Y'], wherein the **third heater array** [e.g., 3M] and **first heater array** [e.g., 3M'] sandwich the **first ink via** [e.g., 2M, Fig. 7] and the **fourth heater array** [e.g., 3Y'] and the **second heater array** [e.g., 3Y] sandwich the **second ink via** [e.g., 2Y, Fig. 7]." Ex. 1007 ¶¶ 131-135.

3. Claim 3

Claim 3 requires "[t]he chip of claim 1, wherein the **first and second ink via** comprise one of a **cyan ink via, a magenta ink via, a yellow ink via, and monochrome ink via**," which Hayasaki discloses. Ex. 1007 ¶¶ 136-138.

Hayasaki teaches "**ink channel 2M** that supplies **magenta (M) ink**, and an **ink channel 2Y** that supplies **yellow (Y) ink**." Ex. 1004 at [0058]; *see also* [0073, 0085, 0093].

Therefore, Hayasaki discloses "[t]he chip of claim 1, wherein the **first** [e.g., ink channel 2M] and **second ink via** [e.g., ink channel 2Y] comprise one of a cyan ink via, a magenta ink via, a yellow ink via, and monochrome ink via." Ex. 1007 ¶¶ 136-138.

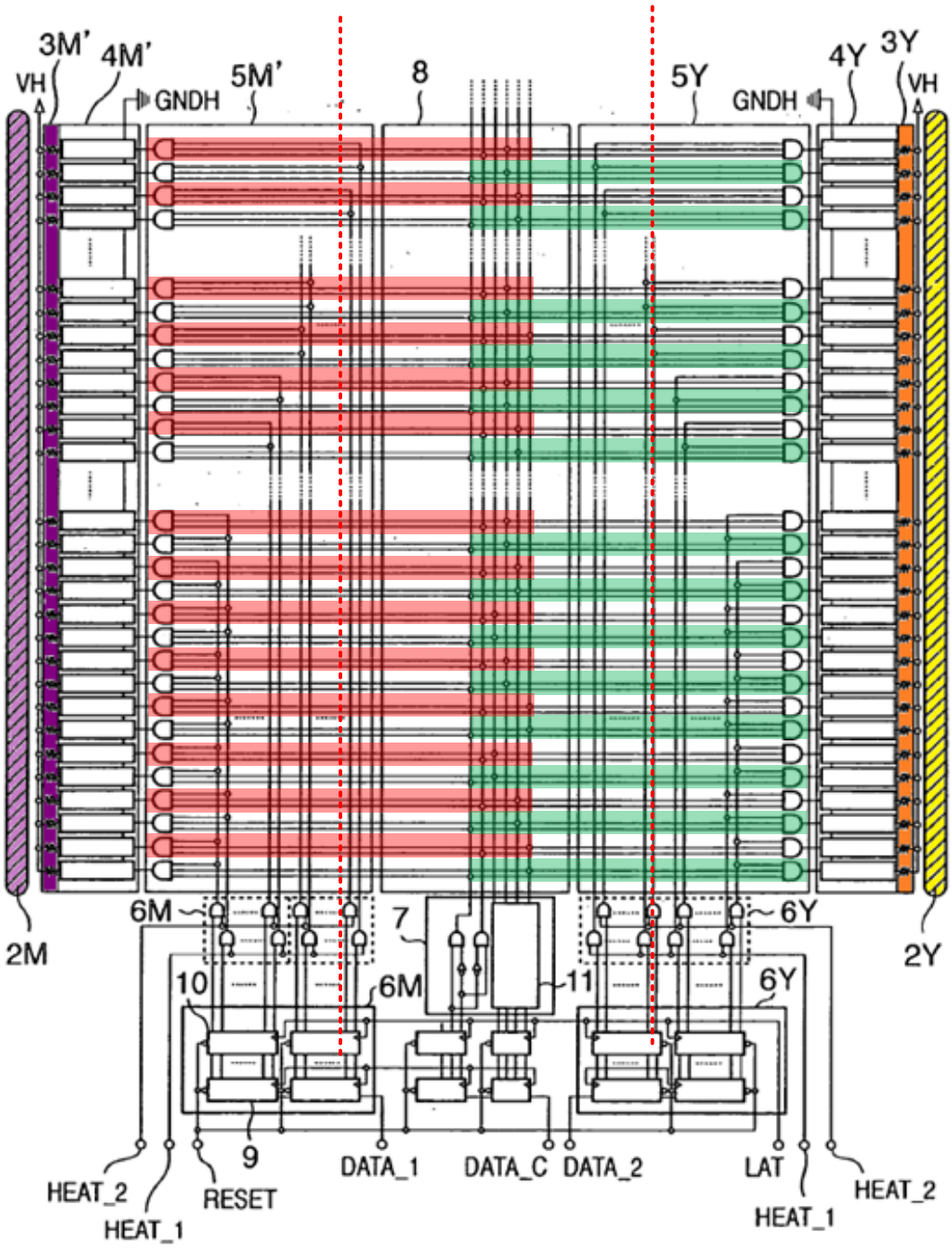
4. Claim 4

Claim 4 requires "[t]he chip of claim 1, wherein the at least one logic array includes **a first logic array for addressing the first heater array** and **a second logic array for addressing the second heater array**, wherein the first logic array is **substantially parallel** to the second logic array," which Hayasaki discloses. Ex. 1007 ¶¶ 139-147.

"[A] first logic array" should be construed to mean "a first group of logic cells," and the term "a second logic array" should be construed to mean "a second group of logic cells." *See* Section VIII.

As noted in Section IX.A.1.f, incorporated here, Figure 9 of Hayasaki shows the at least one logic array (AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8) includes a first set of logic cells (red boxes in Fig. 9) for addressing and controlling the first heater array (3M') and a second set of logic cells (green boxes in Fig. 9) for addressing and controlling the second heater array (3Y).

FIG. 9

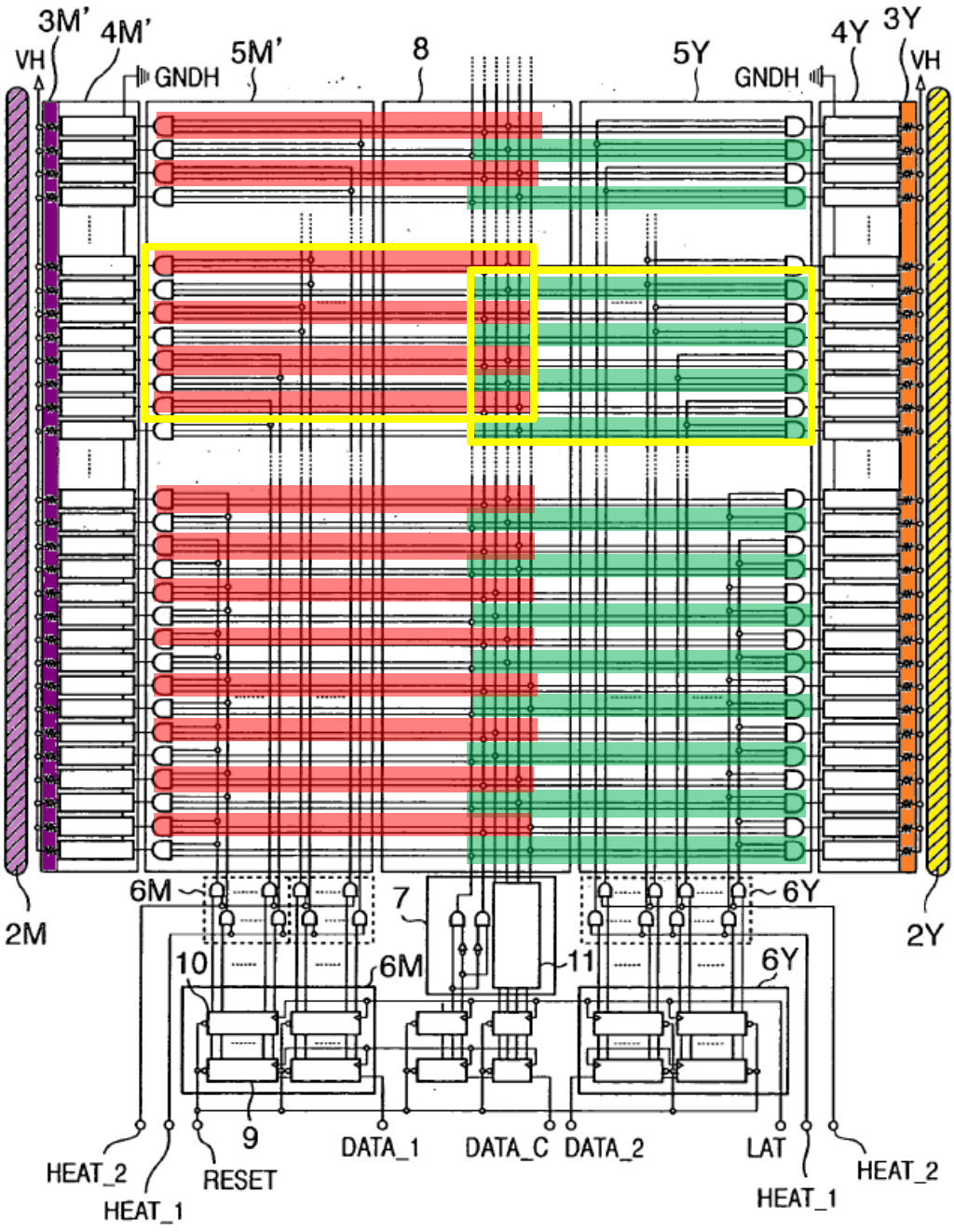


Ex. 1004 at Fig. 9.

These first logic cells (red boxes) and second logic cells (green boxes) correspond to the claimed "first logic array" and "second logic array," respectively because they are a "first group of logic cells" and a "second group of logic cells," respectively. The first group of logic cells and second group of logic cells are also "substantially parallel" to each other. Ex. 1004 at Fig. 9; Ex. 1007 ¶ 142.

To the extent the terms "a first logic array" and "a second logic array" must be defined differently than the terms in claim 1 requiring "a first and a second set of logic cells," Hayasaki still discloses this element. Ex. 1007 ¶ 143. As depicted below, taking a subset of each of the first logic cells (yellow rectangle on the left) and second logic cells (yellow rectangle on the right) can be categorized as a "first group" and "second group," respectively, with them being "substantially parallel" to each other. Ex. 1007 ¶ 143.

FIG. 9



Ex. 1004 at Fig. 9.

Hayasaki also discloses that "a first logic array [is] for addressing the first heater array and a second logic array [is] for addressing the second heater array" for the reasons discussed above in IX.A.1.f, incorporated here.

Therefore, Hayasaki discloses "[t]he chip of claim 1, wherein the **at least one logic array** [e.g., AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8] includes a **first logic array** [e.g., red boxes in Fig. 9 above] for addressing the **first heater array** [e.g., printing element array 3M'] and a **second logic array** [e.g., green boxes in Fig. 9 above] for addressing the **second heater array** [e.g., 3Y], wherein the first logic array is **substantially parallel** to the second logic array [e.g., Fig. 9]." Ex. 1007 ¶¶ 139-147.

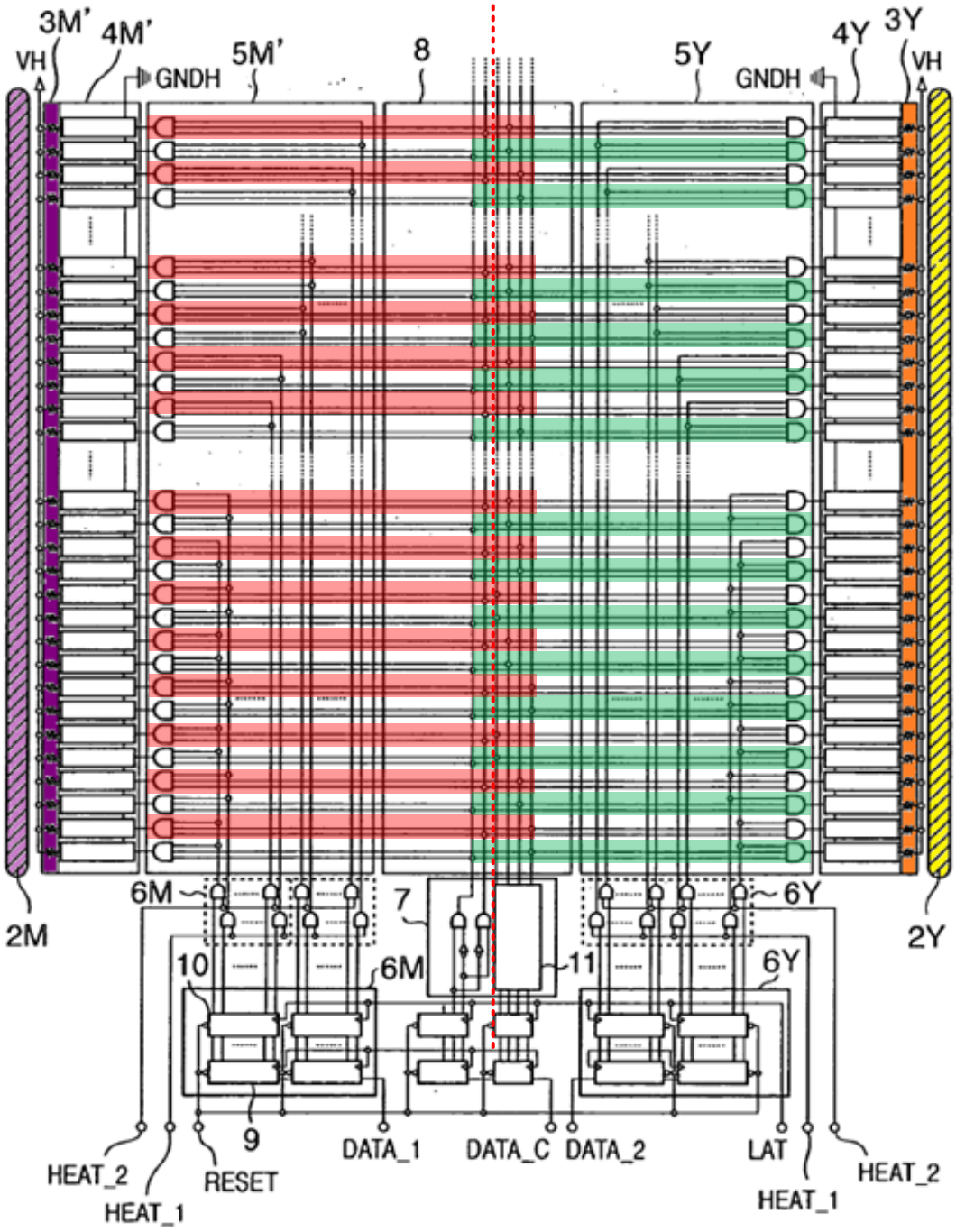
5. Claim 5

Claim 5 requires "[t]he chip of claim 1, wherein the at least one logic array comprises a **single logic array** having **first logic cells for addressing the first heater array** and **second logic cells for addressing the second heater array**, wherein the single logic array is **substantially linear**," which Hayasaki discloses. Ex. 1007 ¶¶ 148-153.

As discussed above in Section IX.A.1.f, incorporated here, Figure 9 of Hayasaki shows the at least one logic array (AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8)

includes first logic cells (red boxes in Fig. 9) for addressing the first heater array and second logic cells (green boxes in Fig. 9) for addressing the second logic array. Ex. 1007 ¶ 150.

FIG. 9



Ex. 1004 at Fig. 9.

The combination of the first logic cells and second logic cells correspond to the claimed "single logic array" as that term would be understood according to its plain and ordinary meaning. Ex. 1007 ¶ 150. Moreover, as seen in Figure 9 above, the single logic array is **substantially linear**. Ex. 1007 ¶ 151.

Therefore, Hayasaki discloses "[t]he chip of claim 1, wherein the at least one logic array comprises a single logic array having first logic cells for addressing the first heater array and second logic cells for addressing the second heater array, wherein the single logic array is substantially linear." Ex. 1007 ¶¶ 148-152.

6. Claim 6

Claim 6 requires "[t]he chip of claim 5, wherein at least **a portion of the first logic cells are interleaved with at least a portion of the second logic cells**, thereby making the single logic array **non-contiguous**," which Hayasaki discloses as explained in IX.A.1.f, incorporated here. Ex. 1007 ¶¶ 153-155.

7. Claim 7

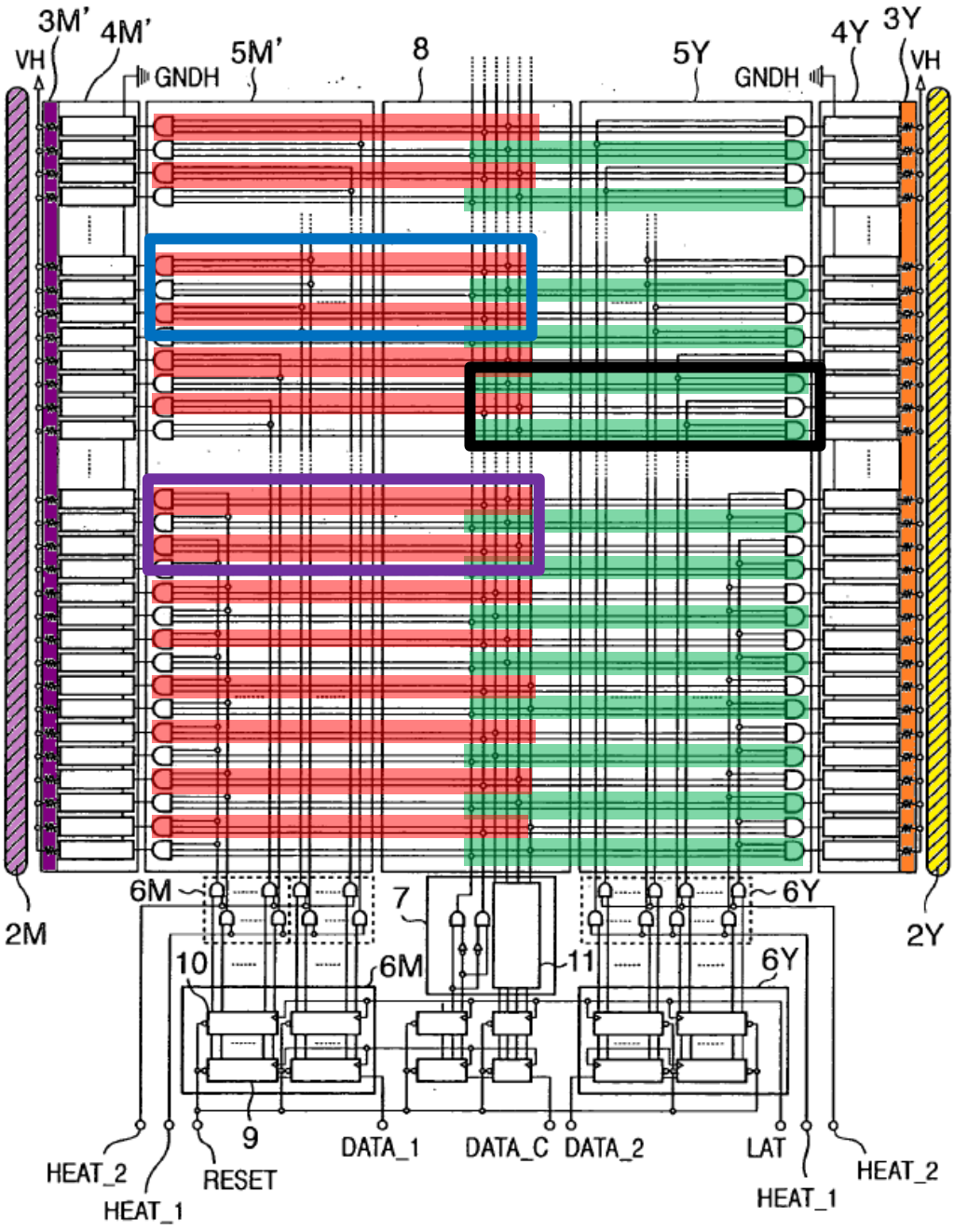
Claim 7 requires "[t]he heater chip [of] claim 6, wherein **a pair of second logic cells** is **interleaved** between a **first pair of first logic cells** and a **second pair of first logic cells**," which Hayasaki discloses. Ex. 1007 ¶¶ 156-160.

The plain language of the claim requires only that a "pair" of second logic cells be "interleaved" between a "first pair" of first logic cells and a "second pair" of first logic cells. There is no further specificity limiting how one should define

these claimed "pair[s]" of cells. The word "pair" is understood based on its plain and ordinary meaning to refer to two. Ex. 1007 ¶m 158.

As seen below, a **pair of second logic cells (green highlights in black box)** is interleaved between a **first pair of first logic cells (red highlights in blue box)** and a **second pair of first logic cells (red highlights in purple box)** because the pair of second logic cells (black box) is placed or inserted between the location of the two sets of pairs of first logic cells (blue and purple boxes) thus making them "interleaved." Ex. 1007 ¶¶ 158-159.

FIG. 9



Ex. 1004 at Fig. 9.

.

Therefore, Hayasaki discloses "[t]he heater chip [of] claim 6, wherein a pair of second logic cells is interleaved between a first pair of first logic cells and a second pair of first logic cells." Ex. 1007 ¶¶ 156-160.

8. Claim 8

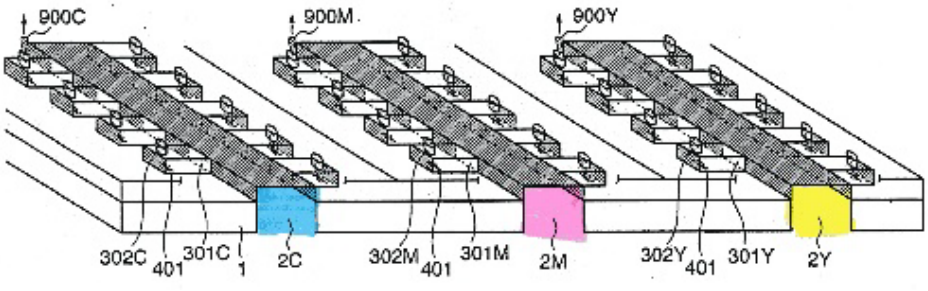
a. 8[P]: "An integrated multi-via heater chip"

Generally, the preamble is not limiting. To the extent the preamble is a limitation of the claim, Hayasaki discloses it." Ex. 1007 ¶¶ 162-166.

In particular, the **tri-color inkjet printhead IJHC** of Hayasaki is the claimed chip for use in a printing device. Ex. 1007 ¶¶ 162-166.

As Hayasaki explains, Figure 3 "is a perspective view showing a three-dimensional structure of a printhead IJHC that discharges **three colors of ink**." Ex. 1004 at [0057].

FIG. 3



Ex. 1004 at Fig. 3.

Hayasaki explains that in Figure 3, "reference numeral 1 denotes a printhead substrate (hereinafter referred to as a "head substrate") on which are formed

electrothermal transducers and the variety of circuits that drive the electrothermal transducers . . . a memory, a variety of pads that form the electrical contacts with the carriage HC, and a variety of signal wires." Ex. 1004 at [0060]. Multiple vias, including **ink channels 2C (cyan), 2M (magenta), and 2Y (yellow),** are placed on the printhead. Ex. 1004 at Fig. 3, [0058].

Therefore, Hayasaki discloses an "**integrated multi-via heater chip** [e.g., printhead chip IJHC]." Ex. 1007 ¶¶ 162-166.

b. 8[A]: "a first heater array having a left side and a right side"

Hayasaki discloses this limitation for the same reasons as described in Section IX.A.1.b, incorporated here.

c. 8[B]: "a first ink via positioned on the left side of the first heater array"

Hayasaki discloses this limitation for the same reasons as described in Section IX.A.1,c, incorporated here.

d. 8[C]: "a second heater array having a left side and a right side, wherein the first heater array and the second heater array are positioned opposite one another so that the right side of the first heater array is facing the left side of the second heater array"

Hayasaki discloses this limitation, including that the first heater array (3M') and second heater array (3Y) are positioned opposite one another (e.g., Fig. 9), for

the same reasons as described in Section IX.A.1.d, incorporated here. *See also* Ex. 1007 ¶¶ 176-180.

e. 8[D]: "a second ink via positioned on the right side of the second heater array"

Hayasaki discloses this limitation for the same reasons as described in Section IX.A.1.e, incorporated here.

f. 8[E]: "a first logic array positioned substantially between the first heater array and the second heater array, wherein the first logic array includes a plurality of first logic cells for addressing and controlling the first heater array and a plurality of second logic cells for addressing and controlling the second heater array, the plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement which allows the first ink via and second ink via to be simultaneously controlled by the first logic array"

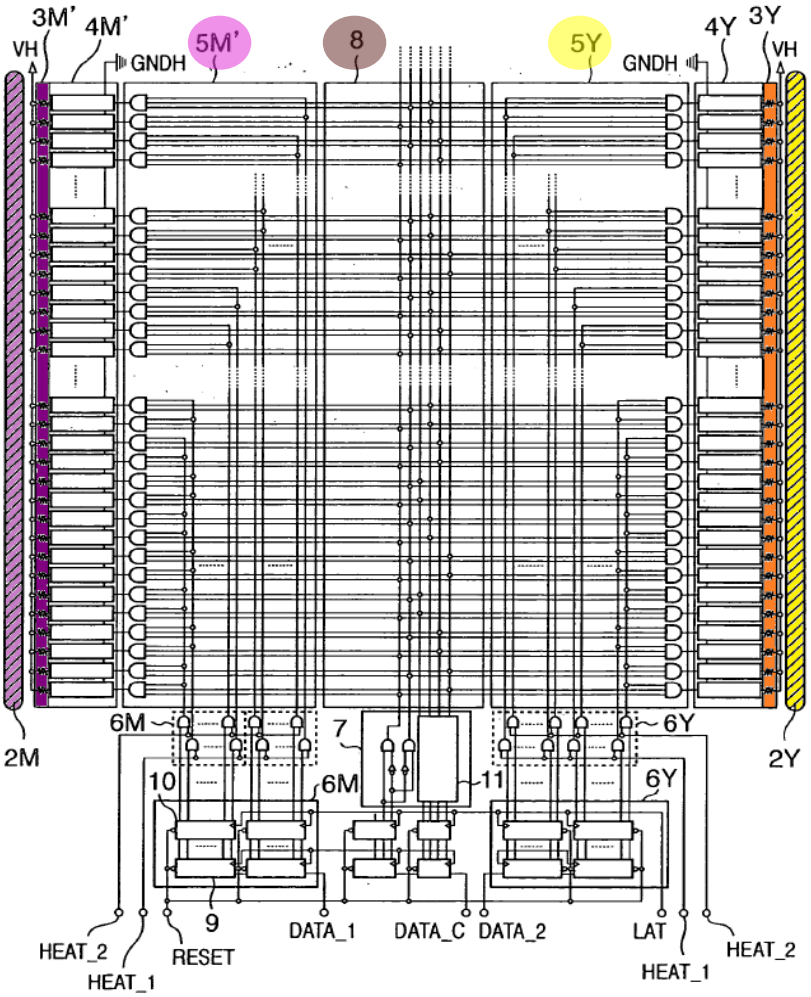
Hayasaki discloses this limitation. Ex. 1007 ¶¶ 185-206.

(i) 8[E], Part 1: "a first logic array positioned substantially between the first heater array and the second heater array"

The term "a first logic array" should be construed to mean "a first group of logic cells." *See* Section VIII. As seen in Figure 9, Hayasaki discloses the claimed group of logic cells that address and control the respective heater arrays, including (i) **the AND circuit array 5M' (purple circle) and its respective portion of the wiring 8 (brown circle), and (ii) the AND circuit array 5Y (yellow circle) and its**

respective portion of the wiring 8 (brown circle), which collectively correspond to **the claimed "first logic array**." Ex. 1007 ¶ 187.

FIG. 9



Ex. 1004 at Fig. 9.

As discussed in Section IX.A.1.f, incorporated here, Hayasaki describes AND circuit arrays 5M' and 5Y as **providing output logic** and that the wiring 8 "concurrently controls a plurality of printing elements." Ex. 1004 at [009, 0104-0163]. As also described in Section IX.A.1.f, incorporated here, AND circuit arrays

5M' and 5Y each includes multiple AND logic cells. *See, e.g.*, Ex. 1004 at Fig. 9; Ex. 1007 ¶¶ 188-190.

Thus, (i) the AND circuit array 5M' and its respective portion of wiring 8, and (ii) the AND circuit array 5Y and its respective portion of wiring 8, together correspond to the claimed "a first logic array" because they all work together to provide output logic and address and control the plurality of printing elements and can be considered a "first group of logic cells." Ex. 1004 at [0093, 0104-0106]; Ex. 1007 ¶ 191.

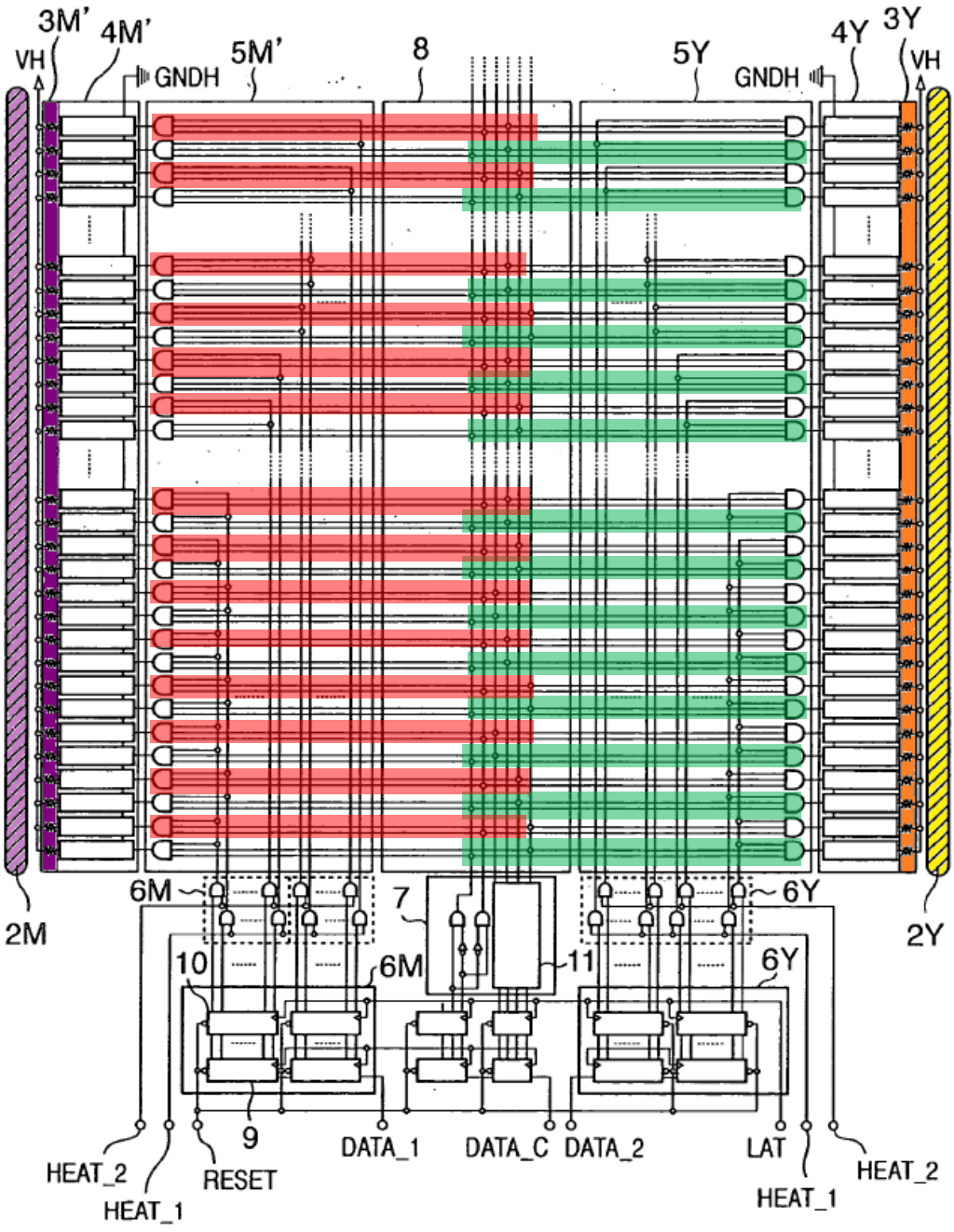
As seen in Figure 9 above, this first logic array (the AND circuit array 5M' (purple circle) and its respective portion of wiring 8 (brown circle) and the AND circuit array 5Y (yellow circle) and its respective portion of wiring 8 (brown circle)) is **positioned substantially between the first heater array (printing element 3M', purple) and the second heater array (printing element 3Y, orange).** Ex. 1007 ¶ 193.

(ii) 8[E], Part 2: "wherein the first logic array includes a plurality of first logic cells for addressing and controlling the first heater array and a plurality of second logic cells for addressing and controlling the second heater array, the plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement which allows the first ink via and second ink via to be

simultaneously controlled by the first logic array"

As discussed in Section IX.A.1.f, incorporated here, the use of the word **"comprising"** in the preamble means **"including but not limited to**." *CIAS,* 504 F.3d at 1360. Thus, **the claim is not restricted to a device that only has interleaved or interlaced logic cells**, i.e., the prior art may disclose other logic cells that are not relevant to the claims.

FIG. 9



Ex. 1004 at Fig. 9.

Given this, as seen in Figure 9 above, Hayasaki discloses a **plurality of first logic cells (red boxes)** and a **plurality of second logic cells (green boxes)** that are

arranged in a **non-contiguous hybrid arrangement** because the plurality of first logic cells (red boxes) are interleaved or interlaced with the plurality of second logic cells (green boxes). *See* Section VIII; Ex. 1007 ¶¶ 194-202.

Hayasaki's disclosure of a plurality of first logic cells in red and a plurality of second logic cells in green interleaved with one another aligns with the plain language of the claim element that does not require **all** of the logic cells within the printhead be interleaved with one another. Therefore, the plurality of first logic cells in red and plurality of second logic cells in green meet the requirement of "the plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement." Ex. 1007 ¶¶ 197-199.

Moreover, Hayasaki also operates its printing elements in an alternating or interleaved manner. Specifically, as Hayasaki explains, in **FIG. 9**, its circuits are configured **so as not to drive adjacent printing elements concurrently**" because "[i]f adjacent printing elements are to be driven concurrently, a phenomenon in which ink is insufficiently supplied adjacent nozzles (i.e., crosstalk) occurs because the inflow and outflow of ink occur at positions near each other." Ex. 1004 at [0095].

Thus, in operation, no adjacent logic cells in each of the AND circuit arrays 5M' and 5Y are operational at the same time to avoid cross-talk phenomenon, which is consistent with the depiction of the claimed plurality of first logic cells (red boxes) and plurality of second logic cells (green boxes). Ex. 1007 ¶¶ 200-202.

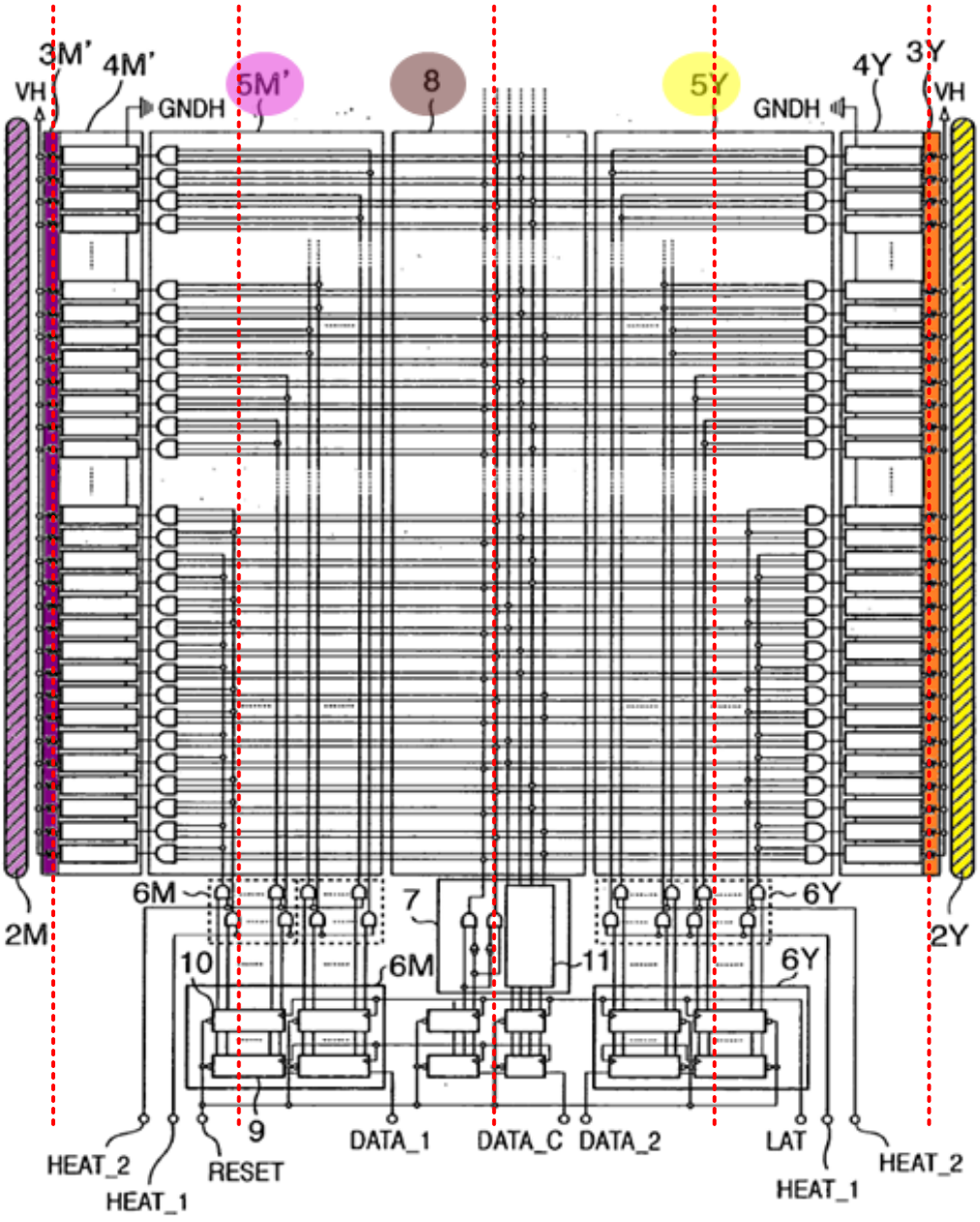
Additionally, for the same reasons as discussed in Section IX.A.1.f, incorporated here, Hayasaki teaches that the plurality of first logic cells (red boxes) addresses and controls the first heater array (3M'), and the plurality of second logic cells (green boxes) addresses and controls the second heater array (3Y) which allows the first ink via (ink channel 2M) and second ink via (ink channel 2Y) to be simultaneously controlled by the first logic array.

Therefore, Hayasaki discloses "a **first logic array** [e.g., AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8] positioned substantially between the **first heater array** [e.g., 3M'] and the **second heater array** [e.g., 3Y], wherein the first logic array includes a **plurality of first logic cells** [e.g., red boxes in annotated Fig. 9 above] for addressing and controlling the first heater array and a **plurality of second logic cells** [e.g., green boxes in annotated Fig. 9 above] for addressing and controlling the second heater array, the plurality of first logic cells and the plurality of second logic cells are arranged in a **non-contiguous hybrid arrangement** [e.g., interleaved as annotated Fig. 9 above] which allows the first ink via and second ink via to be simultaneously controlled by the first logic array." Ex. 1007 ¶¶ 185-206.

g. 8[F]: "wherein the first logic array is substantially parallel with the first heater array and second heater array"

As seen in Figure 9, the first logic array (AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8) is **substantially parallel** with the first heater array (printing element array 3M', purple) and second heater array (printing element array 3Y, orange). Ex. 1007 ¶ 208. This can be seen below with the longitudinal axes for each of the AND circuit array 5M' (purple circle), the wiring 8 (brown circle), the AND circuit array 5Y (yellow circle), the first heater array (3M', purple), and the second heater array (3Y, orange), all being parallel to one another.

FIG. 9



Ex. 1004 at Fig. 9.

Therefore, Hayasaki discloses "wherein the **first logic array** [e.g., AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y

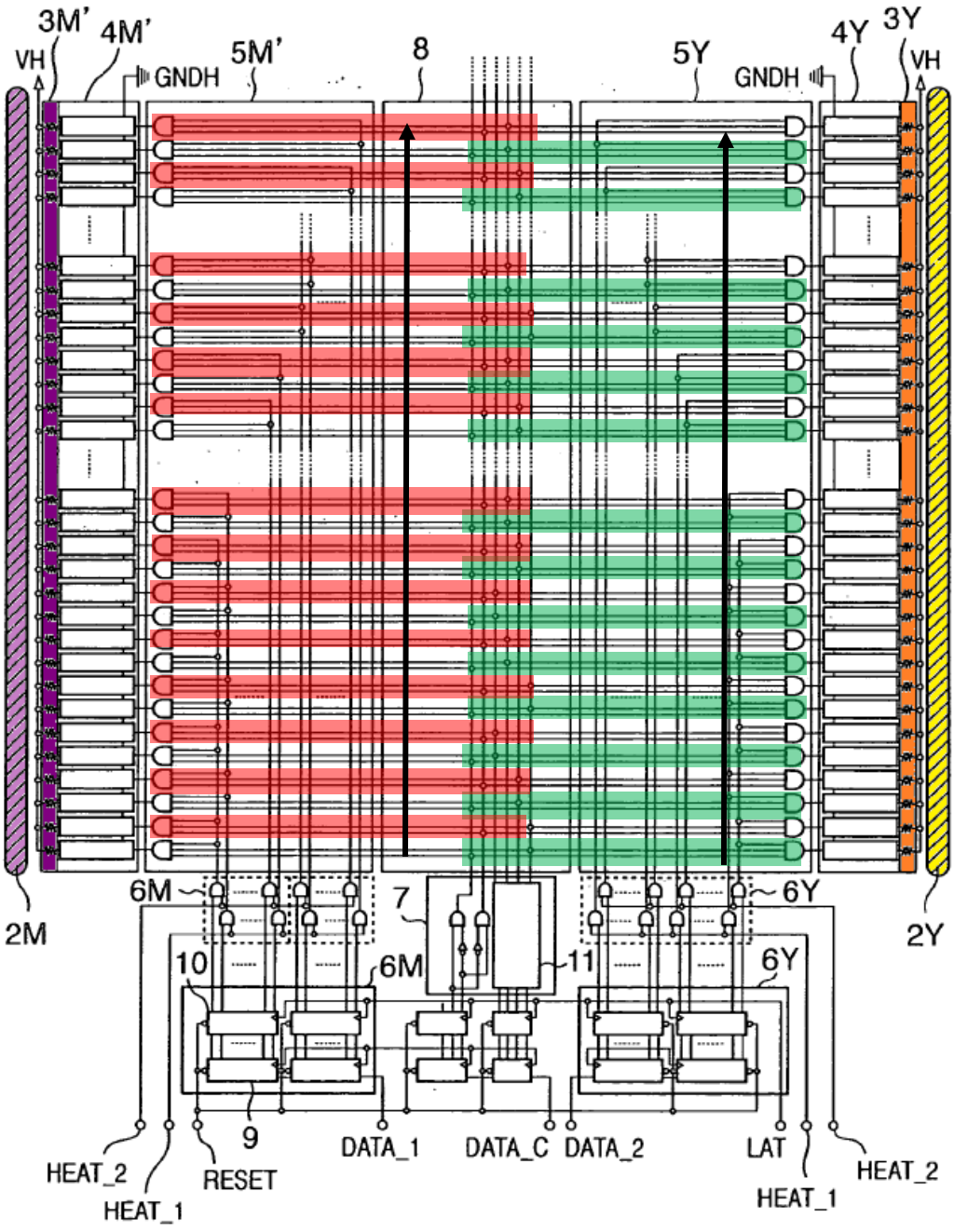
and its respective portion of wiring 8] is substantially parallel with the **first heater array** [e.g., 3M'] and **second heater array** [e.g., 3Y]." Ex. 1007 ¶¶ 207-210.

9. Claim 9

Claim 9 requires "[t]he heater chip of claim 8, wherein at least a portion of the first set of logic cells and at least a portion of the second set of logic cells are **substantially aligned**," which Hayasaki discloses. Ex. 1007 ¶¶ 211-214.

As seen in annotated Figure 9, Hayasaki teaches that at least a portion of the first set of logic cells (red) and at least a portion of the second set of logic cells (green) are substantially aligned because they line up vertically as depicted by the black arrows.

FIG. 9



Therefore, Hayasaki discloses "[t]he heater chip [of] claim 8, wherein at least a portion of the first set of logic cells and at least a portion of the second set of logic cells are **substantially aligned**." Ex. 1007 ¶¶ 211-214.

10. Claim 10

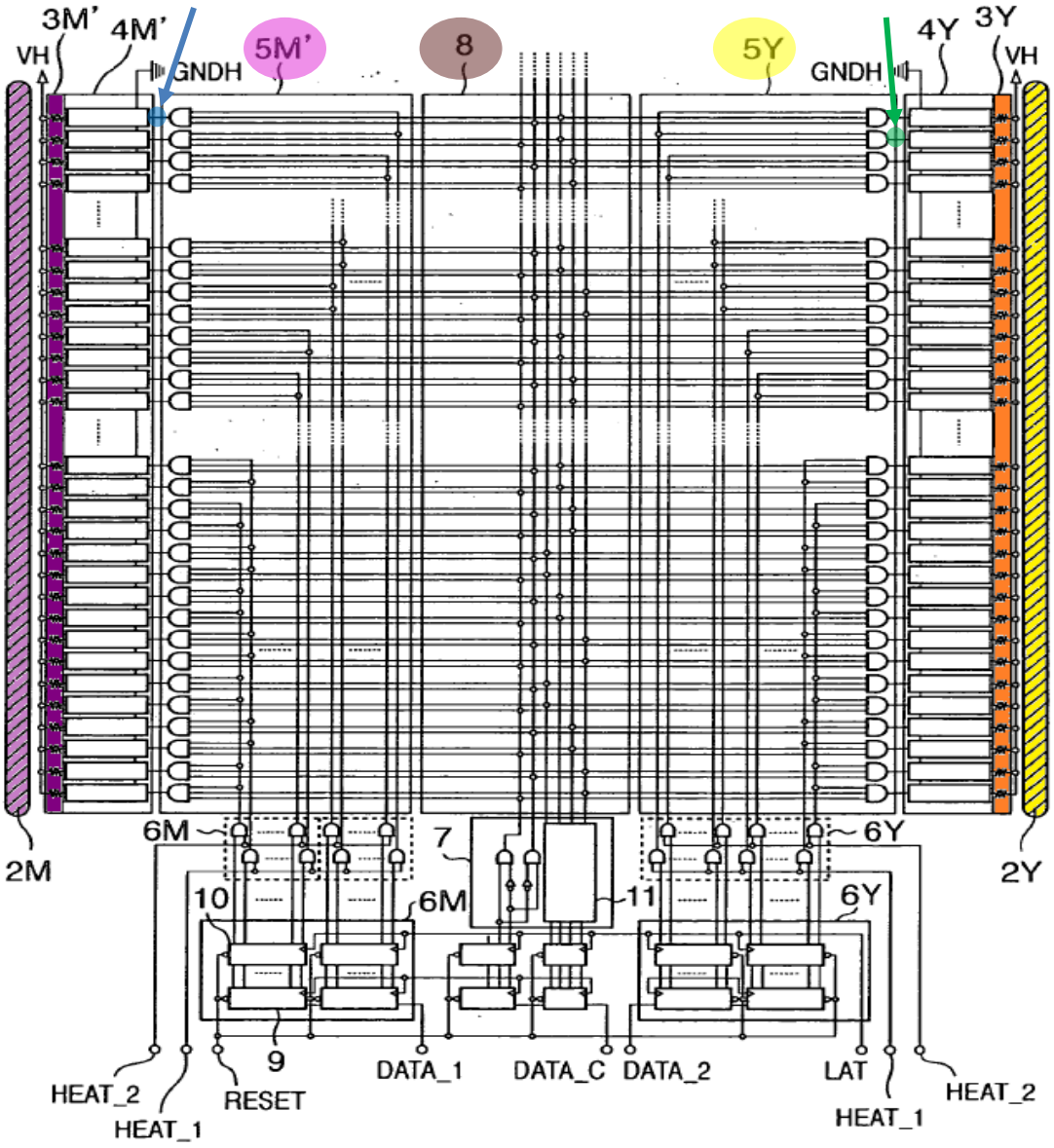
Claim 10 requires "[t]he heater chip of claim 8, wherein the first logic cells are interleaved with the second logic cells," which Hayasaki discloses as described in Section IX.A.8.f, incorporated here.

11. Claim 13

Claim 13 requires "[t]he heater chip [of] claim 8, wherein at least a portion of **control signals for the first logic cells** are **routed between** the **first heater array and the first logic array** and wherein at least a portion of **control signals for the second logic cells** are **routed between** the **second heater array and the first logic array**," which Hayasaki discloses. Ex. 1007 ¶¶ 218-222.

As seen in Figure 9, part of the control signal (blue circle noted by blue arrow) for the first logic cells are routed between the **first heater array** (3M', dark purple) and **first logic array** [AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8]. Part of the control signal (green circle noted by green arrow) for the second logic cells is routed between the **second heater array** (3Y, orange) and **first logic array**. Ex. 1007 ¶ 221.

FIG. 9



Ex. 1004 at Fig. 9.

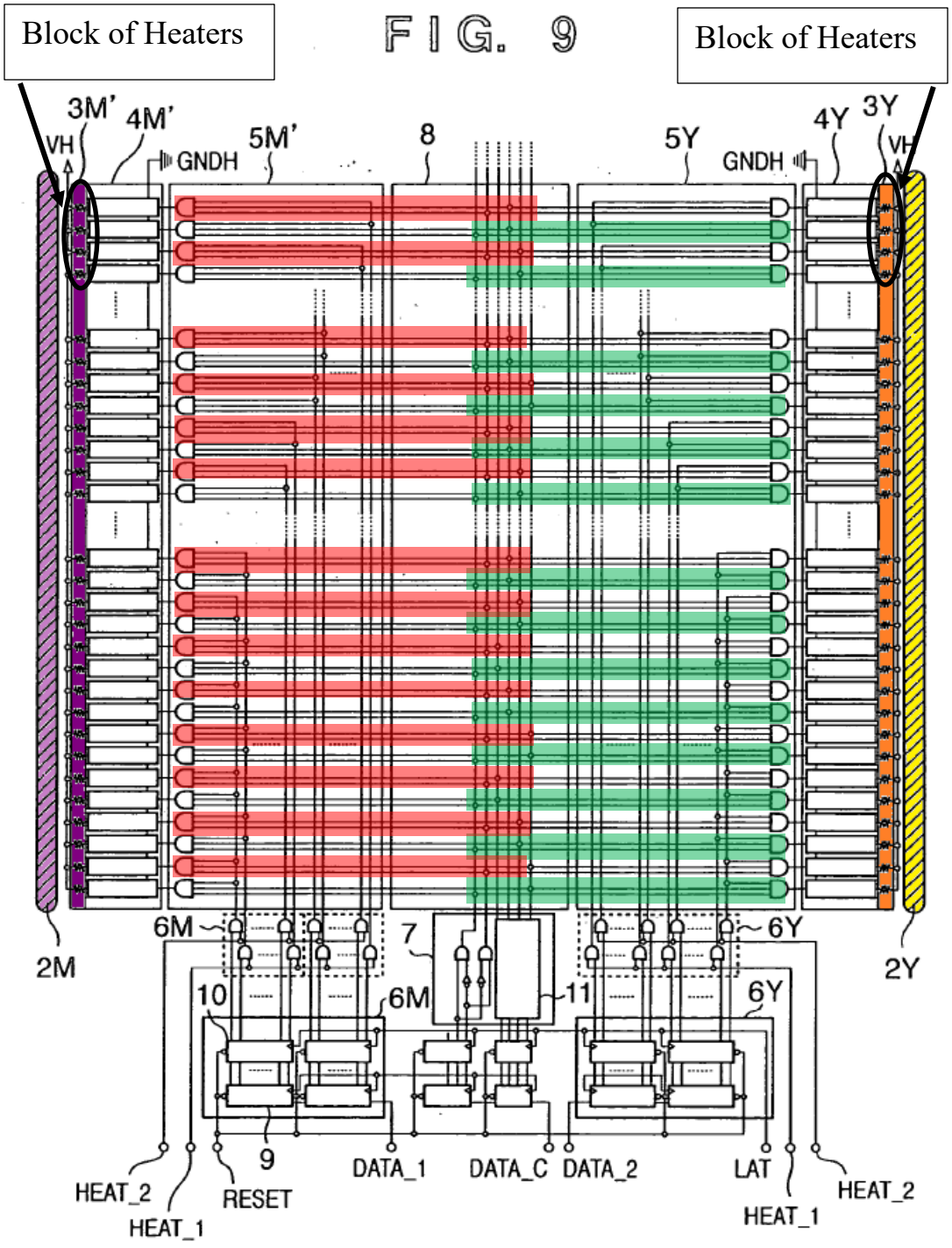
Therefore, Hayasaki discloses "[t]he heater chip [of] claim 8, wherein at least a portion of control signals for the first logic cells are routed between the first heater array and the first logic array and wherein at least a portion of control signals for the

second logic cells are routed between the second heater array and the first logic array." Ex. 1007 ¶¶ 218-222.

12. Claim 14

Claim 14 requires "[t]he heater chip of claim 8, wherein the **first heater array** comprises a **plurality of blocks of heaters** and the **second heater array** comprises a plurality of **blocks of heaters**, wherein each block of heaters in the first heater array is addressed by at least a portion of the first logic cells and wherein each block of heaters in the second heater array is addressed by at least a portion of the second logic cells," which Hayasaki discloses. Ex. 1007 ¶¶ 223-230.

In Figure 9 below, the first heater array (3M', purple) comprises a plurality of blocks of heaters because each individual resistor within 3M' constitutes a heater with a set of these resistors (as depicted by the elongated black circle) constituting a block of heaters. Ex. 1007 ¶ 225. Similarly, the second heater array (3Y, orange) also comprises a plurality of blocks of heater because each individual resistor within 3Y constitutes a heater with a set of these resistors (as depicted by the elongated black circle) constituting a block of heaters. Ex. 1007 ¶ 226.



Ex. 1004 at Fig. 9.

Hayasaki also teaches that each of the blocks of heaters in the first heater array (3M', purple) is addressed by at least a portion of the first logic cells (red boxes),

and each block of heaters in the second heater array (3Y, orange) is addressed by at least a portion of the second logic cells (green).

As Hayasaki explains:

> The ink channels 2M and 2Y are respectively connected to the printing element arrays 3M' and 3Y, in turn, respectively connected to the driver arrays 4M' and 4Y, and in turn, respectively connected to **control wires and AND circuit arrays 5M' and 5Y that enable individual control of these elements. Depending on the output logic of each of the AND circuit arrays 5M' and 5Y**, the driver arrays 4M' and 4Y are driven individually so as to print. That is, an electric current that causes ink discharge is sent **through the relevant printing elements of the printing element arrays 3M' and 3Y**.

Ex. 1004 at [0093].

Hayasaki also explains in the Background of the Invention that "a configuration is known that provides a concurrently drivable control wiring terminal that places N printing elements on one block and the printing elements are powered during a period in which the terminal is activated so as to enable printing onto the printing medium." Ex. 1004 at [0004]. Hayasaki further explains that "a configuration is known that mounts several or even tens of concurrently drivable drive integrated circuits, placing N printing elements on one block, on a single substrate and aligning image data with the printing elements so as to enable printing onto the printing medium." Ex. 1004 at [0005].

As Hayasaki explains, "reference numeral 7 denotes a circuit that time-divisionally drives groups of printing elements that are selectively controlled individually by control circuits 6C, 6M and 6Y, and ordinarily is comprised of a decoder circuit and a shift register circuit." Ex. 1004 at [0078]. "[T]he control wires are laid so as to provide shared control over the plurality of printing element arrays 3C and 3C', 3M and 3M', and 3Y and 3Y', thus achieving a head substrate area reduction as shown in FIG. 7." Ex. 1004 at [0087]; *see also* [0125].

Therefore, Hayasaki discloses "[t]he heater chip of claim 8, wherein the **first heater array** [e.g., 3M'] comprises a **plurality of blocks of heaters** [e.g., annotated Fig. 9 above] and the **second heater array** [e.g., 3Y] comprises a **plurality of blocks of heaters** [e.g., annotated Fig. 9 above], wherein each block of heaters in the first heater array is addressed by at least a portion of the first logic cells and wherein each block of heaters in the second heater array is addressed by at least a portion of the second logic cells," which Hayasaki discloses. Ex. 1007 ¶¶ 223-230.

B. Ground #2: Claims 1-10 and 13-14 are rendered obvious by Hayasaki and Silverbrook

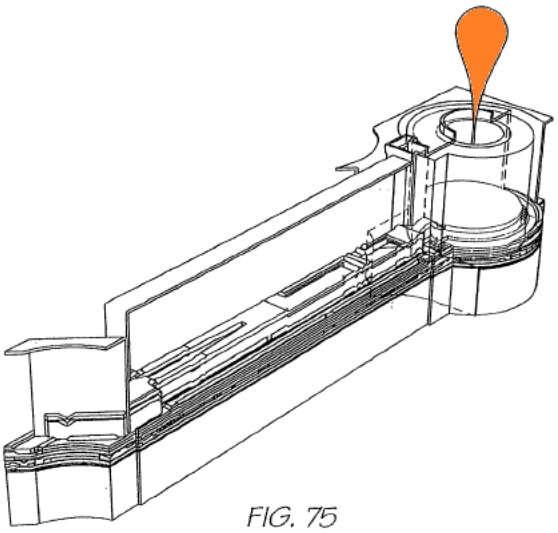
1. Claim 1

For the reasons presented above for Ground 1, claim 1, Hayasaki discloses all of the elements of this claim.

To the extent the Board determines that Hayasaki does not disclose the claimed "first and second set of logic cells arranged in a **non-contiguous hybrid**

arrangement," then this element is clearly described in Silverbrook. Ex. 1007 ¶¶ 232-245.

As in the '629 Patent and Hayasaki, Silverbrook describes an inkjet printhead including control logic. Figure 75 of Silverbrook "illustrates a side perspective view partly in section of a single nozzle ejecting ink [orange]." Ex. 1005 at [0184].



Ex. 1005 at Fig. 75.

Figure 76 of Silverbrook below illustrates "a schematic of the control logic for a single nozzle." Ex. 1005 at [0185, 0300]. Silverbrook notes "[t]he **control logic 280** [red] is utilized to **activate a heater element 281** [green] on demand." Ex. 1005 at [0300].

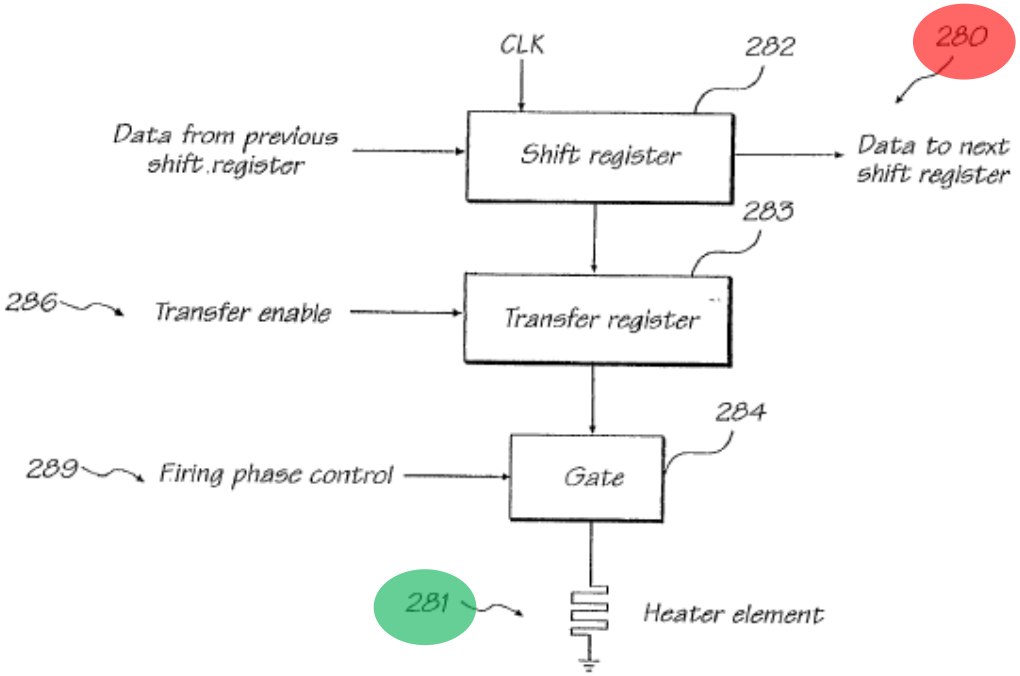


FIG. 76

Ex. 1004 at Fig. 76.

In Figure 77 below, "a CMOS implementation of the control logic of a single nozzle" is depicted. Ex. 1005 at [0186].

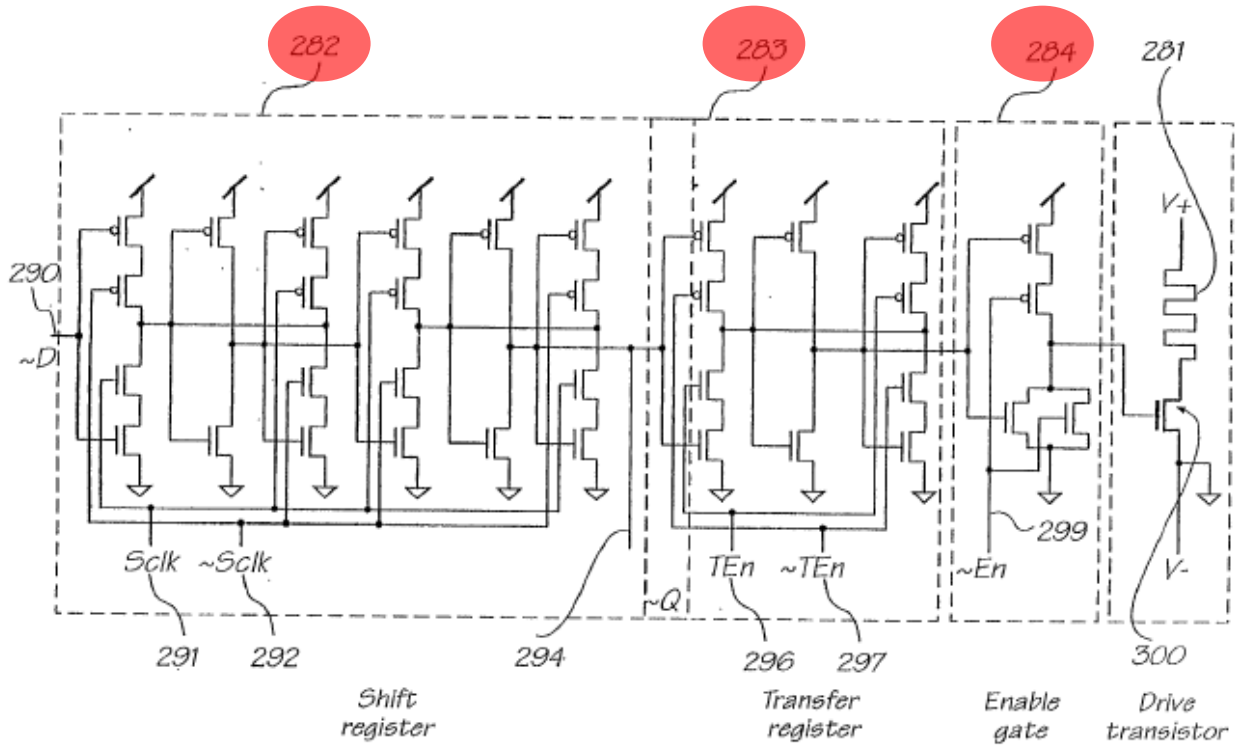


FIG. 77

Ex. 1004 at Fig. 77.

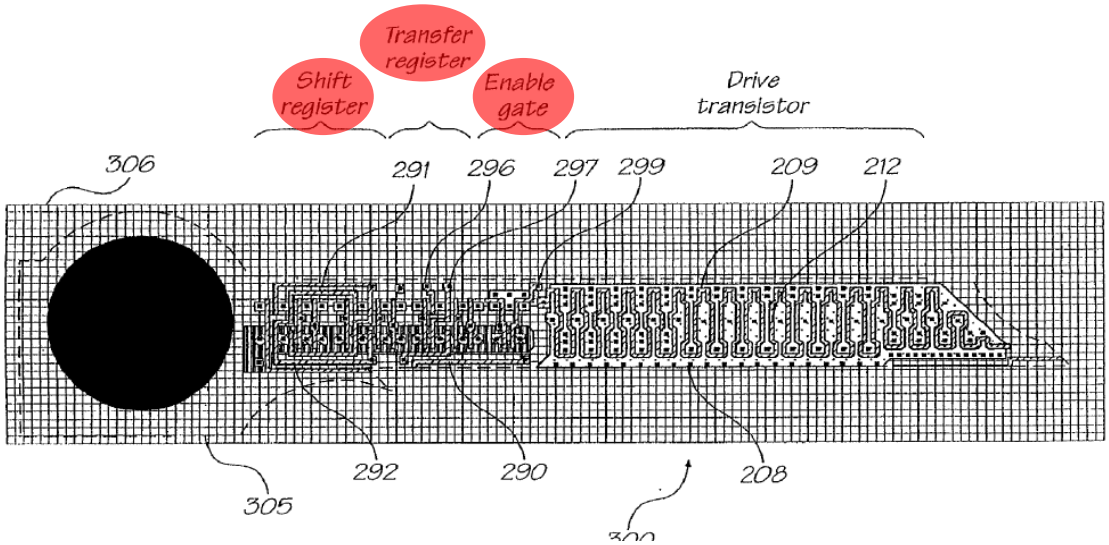
Silverbrook explains that control logic 280 includes "**a shift register 282, a transfer register 283 and a firing control gate 284 [each noted with red circles]**," and that:

> **[S]hift register 282** takes an inverted data input and latches the input under control of shift clocking signals 291, 292. The data input 290 is output 294 to the next shift register and is also latched by a **transfer register 283** under control of transfer enable signals 296, 297. The **enable gate 284 is activated under the control of enable signal 299 so as to drive a power transistor 300 which allows for resistive heating of resistor 281**. The functionality of the **shift register 282, transfer register 283 and enable gate 284 are standard CMOS**

components <u>well understood by those skilled in the art</u> of CMOS circuit design.

Ex. 1005 at Abstract, [0300, 0301].

A "general layout" of the shift register (red) transfer register (red), and firing control gate or enable gate (red) of the control logic 280 placed in a unit cell 305 is presented in Figure 79 with Silverbrook noting that "[t]he ink jet print head can consist of a large number of replicated unit cells each of which has basically **the same design**." Ex. 1005 at [0303]. As seen in Figure 79 below, the logic is placed adjacent the nozzle (black circle). Thus, in Silverbrook the shift register, transfer register, and enable gate (all in red), together form a logic cell. Ex. 1007 ¶238.



Ex. 1005 at Fig. 79.

In Figure 85 below, arrays of unit cells of Figure 79 are depicted showing a portion 360 of a [*sic*] array of ink ejection nozzles which are divided into three

groups 361-363 with each group providing separate color output (cyan, magenta and yellow) so as to provide full three color printing." Ex. 1005 at [0311].

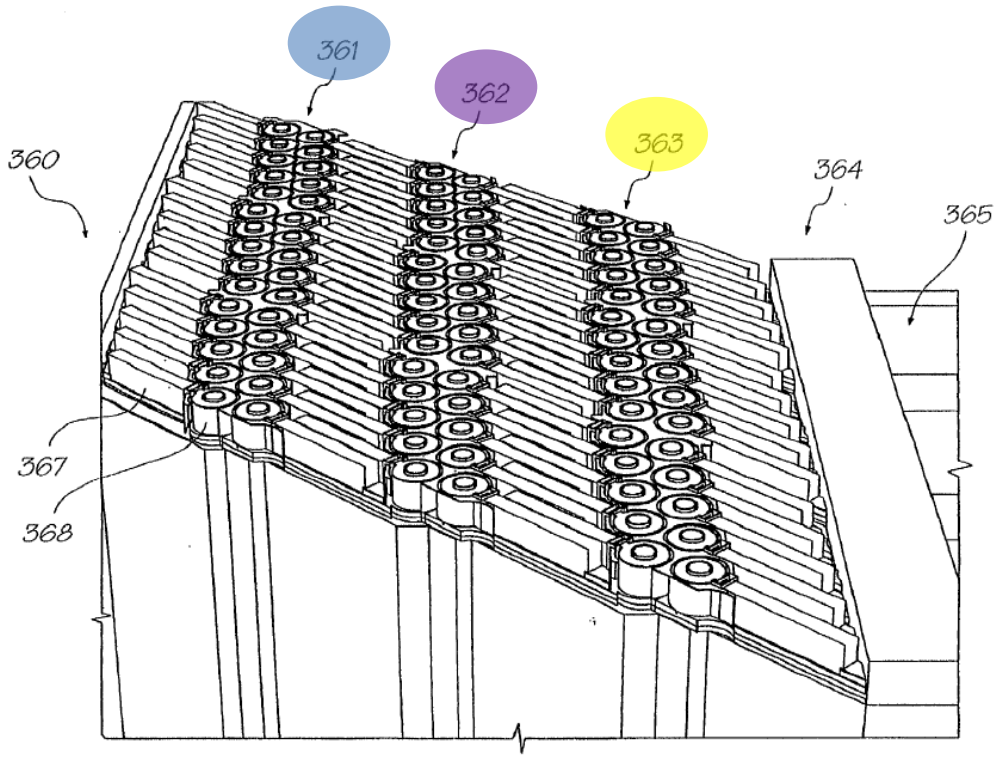


FIG. 85

Ex. 1005 at Fig. 85.

Figure 86 below shows an enlarged view of a portion of Figure 85. As seen below, the logic cells (pink) associated with one group of nozzles (and its associated heaters) is clearly interleaved or interlaced with logic cells (blue) associated with another group of nozzles (and its associated heaters) and thus the sets of logic cells are arranged in a **non-contiguous hybrid arrangement**. Ex. 1007 ¶ 241.

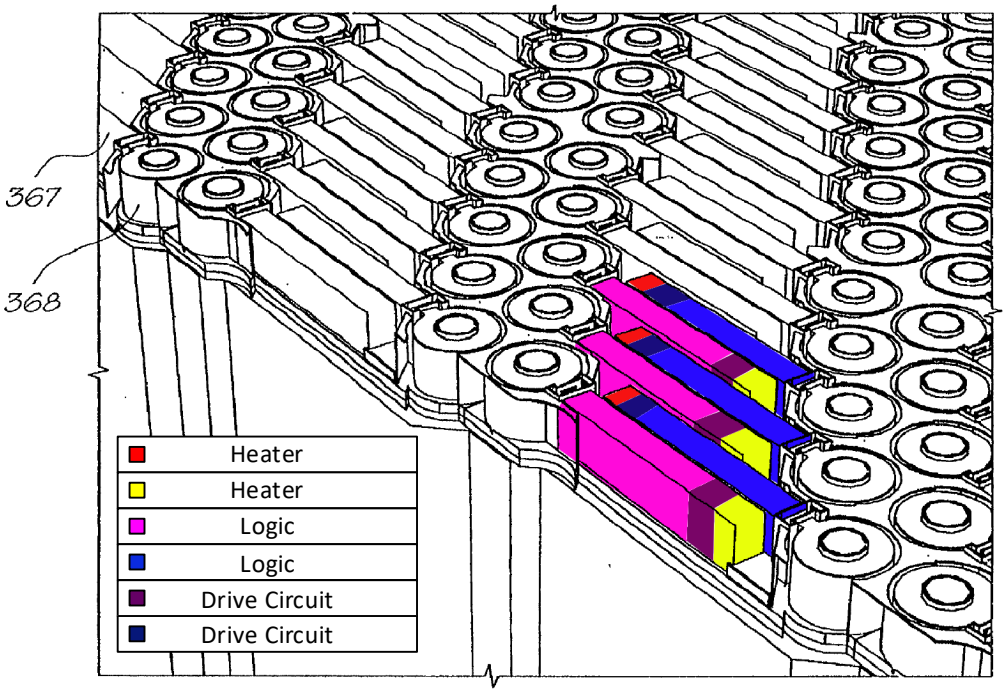


FIG. 86

Ex. 1005 at Fig. 86.

In Silverbrook, the combination of the logic cells (pink and blue) corresponds to the "at least one logic array" of claim 1 placed in a non-contiguous hybrid arrangement because the **logic cells** are **interleaved or interlaced**. This at least one logic array includes **first logic cells** (purple) and **second logic cells** (blue) with each set addressing and controlling its respective heater array (yellow, red). Ex. 1005 at Fig. 76, [0300]; Ex. 1007 ¶ 242. Silverbrook also discloses that nozzles from each color in the printhead fire simultaneously and thus are simultaneously controlled by the at least one logic array. Ex. 1005 at [0341].

A POSITA would have understood that placing the logic cells in this arrangement provides a more compact printhead because it decreases the width of

the printhead needed to contain the sets of logic cells, and it would have therefore been obvious to a POSITA to modify Hayasaki's logic cells to be interleaved or interlaced with one another as described in Silverbrook or replace Hayasaki's logic cells with Silverbrook's interleaved/interlaced logic cells to reduce printhead size. Ex. 1007 ¶ 243.

As such, a POSITA would have understood that Hayasaki as modified by Silverbrook discloses "**at least one logic array** [e.g., Hayasaki's AND circuit array 5M' and its respective portion of wiring 8 and AND circuit array 5Y and its respective portion of wiring 8 modified per Silverbrook's pink and blue logic cell layout in Fig. 86 above, or Hayasaki's circuit arrays 5M' and 5Y' replaced by Silverbroook's logic cells as shown in Fig. 86 above] including a **first** [logic set], [e.g., the AND logic in Hayasaki 5M'and associated wiring in 8 modified/replaced by Silverbrook's pink cells in Fig. 86 above] and a **second set of logic cells** [e.g., the AND logic in Hayasaki 5Y and associated wiring in 8 modified/replaced by Silverbrook's blue cells in Fig. 86 above] arranged in a **non-contiguous hybrid arrangement** [e.g., interleaving Hayasaki's first and second set of logic cells as modified by the teachings in Figs. 85-86 of Silverbrook or replacing Hayasaki's logic cells with those of Silverbrook], the at least one logic array is disposed substantially between the **first heater array** [e.g., Hayasaki's printing element array 3M' modified/replaced by the yellow heater array in Silverbrook shown in Fig. 86

above] and the **second heater array** [e.g., Hayasaki's printing element array 3Y modified/replaced by the red heater array in Silverbrook shown in Fig. 86 above] wherein the first set of logic cells addresses and controls the first heater array and the second set of logic cells addresses and controls the second heater array, which allows the first ink via and second ink via to be simultaneously controlled by the at least one logic array."

a. Motivation to Combine Hayasaki and Silverbrook

A POSITA would have been motivated to modify the printhead chip of Hayasaki to place the first and second sets of logic cells in a non-contiguous hybrid arrangement as described by Silverbrook and would have had a reasonable expectation of success in making such a modification. Ex. 1007 ¶¶ 246-255.

First, Hayasaki and Silverbrook are **analogous** to the claimed subject matter in the '629 Patent as they all are within the **same field of endeavor**—inkjet printheads. Ex. 1001 at Abstract; Ex. 1004 at Abstract; Ex. 1005 at Abstract. Although Hayasaki describes a different mechanism for discharging the ink than Silverbrook (a heater activated bubble jet system as compared to a heater activated actuator arm system), the circuitry (including the logic cells and heaters) is practically identical. Ex. 1007 ¶ 249.

Moreover, both Hayasaki and Silverbrook describe their respective inkjet printheads as being used in similar inkjet printers. Hayasaki describes an inkjet

printer IJRA that can utilize its described printheads. Ex. 1004 at Fig. 1, [0049, 0055, 0057]. Hayasaki also notes that it's teachings "can be applied to other types of inkjet printing methods." Ex. 1004 at [0128]. Silverbrook explains "the presently disclosed ink jet printing technology is suited to a **wide range** of printing systems," including (i) color and monochrome office printers, home PC printers, etc. Ex. 1005 at [0539-0589]. Additionally, the USPTO classified all three under the same classification number—U.S. Cl. 347. Ex. 1001 at 1; Ex. 1004 at 1; Ex. 1005 at 1.

Each of Hayasaki and Silverbrook also seek to **address a similar problem** as the '629 Patent—providing a smaller printhead. Ex. 1007 ¶ 250. The '629 Patent explains "there is a need in the industry for heater chips that can provide for enhanced printing resolutions while **reducing chip die sizes**." Ex. 1001 at 1:42-44. Hayasaki explains "the present invention is **conceived as a response to**" "disadvantages of the conventional art" and notes the invention provides a printhead substrate "capable of controlling the driving of a larger number of printing elements **in a reduced surface area**." Ex. 1004 at [0003-0024]. Silverbrook also notes that "[m]ost modern CMOS processes achieve high yield with chip areas in excess of 1cm^2" but "[t]here is a strong incentive to ensure that the chip area is less than 1 cm^2." Ex. 1005 at [0463].

As such, a POSITA would have considered Hayasaki and Silverbrook as **analogous art**. Ex. 1007 ¶ 250.

Second, a POSITA would have been **motivated** to further reduce the size of Hayasaki's printhead by interleaving or interlacing Hayasaki's logic cells as taught by Silverbrook, or alternatively simply replacing Hayasaki's logic cells with those of Silverbrook. Ex. 1007 ¶ 251. As Silverbrook explains, its invention provides a "Small Total Print head Size." Ex. 1005 at [0458-0459]. Silverbrook further explains that "[t]here is a strong incentive to ensure that the chip area is less than 1 cm^2" partly because "[c]ost increases rapidly between 1cm^2 and 4 cm^2, with chips larger than this rarely being practical." Ex. 1005 at [0463]. Silverbrook continues noting that for "thermal ink jet and Bubblejet print heads, the chip width is typically around 5 mm, limiting the cost effective chip length to around 2 cm," and thus a goal of the invention is "to **reduce the chip width** as much as possible."

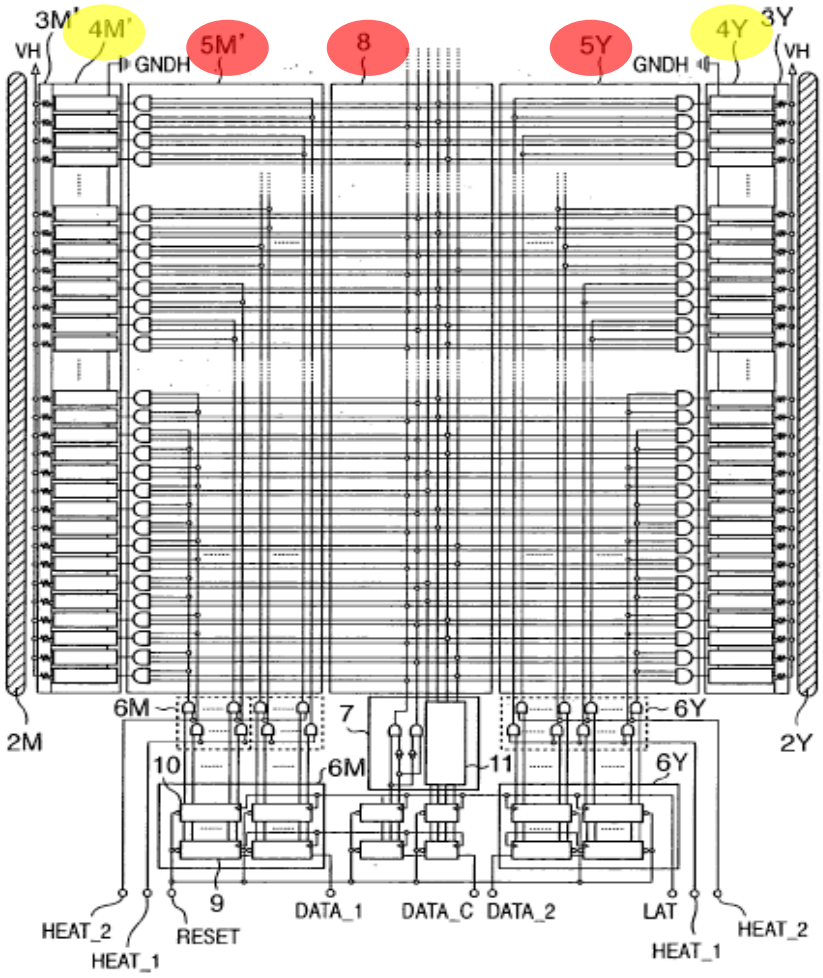
A POSITA would have understood that at least some of this reduced chip size in Silverbrook derives from its placement of the logic cells in an interleaved pattern as in Figure 86 because it decreases the space required for all of the logic circuitry of the printhead. Ex. 1007 ¶ 253. Thus, a POSITA would have been motivated to either interleave Hayasaki's logic cells as taught by Silverbrook, or alternatively replace Hayasaki's logic cells with those of Silverbrook to obtain this decreased chip size. Ex. 1007 ¶ 253.

Thus, a POSITA would have been motivated to modify the layout of Hayasaki's logic cells as taught by Silverbrook (or replace Hayasaki's logic cells with those of Silverbrook) to further Hayasaki's described advantage of reducing the substrate size and to also decrease printhead manufacturing costs. Ex. 1007 ¶ 253; Ex. 1004 at [0003-0024]. As discussed above, reducing chip sizes is the same problem the '629 Patent seeks to address. Ex. 1001 at 1:42-44; Ex. 1007 ¶ 250.

Finally, a POSITA would have had a reasonable expectation of success in combining Hayasaki with Silverbrook. Ex. 1007 ¶¶ 254-255. Like the '629 Patent, Hayasaki and Silverbrook utilize a thermal actuator to eject droplets of ink and have a drive circuit located adjacent the thermal actuators with logic circuitry placed adjacent the drive circuit. Ex. 1004 at [0059, 0093]; Ex. 1005 at [0225, 0301].

As seen in the comparison of Figure 86 of Silverbrook and Figure 9 of Hayasaki, the circuitry of the two are fundamentally the same with a heater (Hayasaki 3M' and 3Y) placed adjacent drive circuity (Hayasaki 4M' and 4Y) placed adjacent to logic circuitry (Hayasaki 5M', 8, 5Y).

FIG. 9



Ex. 1004 at Fig. 9.

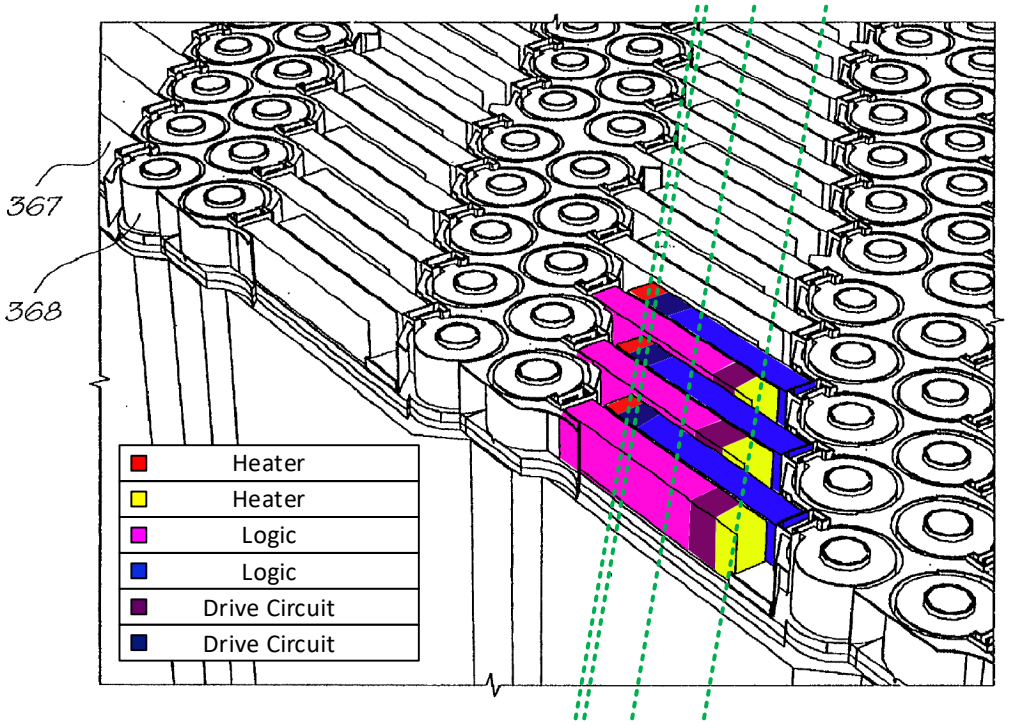


FIG. 86

Ex. 1005 at Fig. 86.

Therefore, a POSITA familiar with Hayasaki would have looked to other inkjet references with similar circuitry (e.g., logic cells, wiring and heaters), like Silverbrook, for teachings on how to adjust the circuitry layout to reduce printhead size and save costs. Such a POSITA would have immediately recognized that the simplicity of Silverbrooks interleaved logic cells could be applied to Hayasaki's circuit array by either modifying Hayasaki consistent with Silverbrook to have a non-contiguous hybrid arrangement of Hayasaki's logic cells or simply replacing Hayasaki's logic cells with those of Silverbrook. Ex. 1007 ¶ 255.

Finally, because this modification/replacement is very simple and only requires changing the circuitry layout, a POSITA would have had a **reasonable expectation of success** that would require no more than routine experimentation to work. Ex. 1007 ¶¶ 254-255.

2. Claims 2-3

For the reasons discussed above in Sections IX.A.2 and IX.A.3 (Ground 1, claims 2-3), incorporated here, Hayasaki discloses the limitations of these claims.

3. Claim 4

Claim 4 requires "[t]he chip of claim 1, wherein the at least one logic array includes **a first logic array for addressing the first heater array** and **a second logic array for addressing the second heater array**, wherein the first logic array is **substantially parallel** to the second logic array." As discussed in Section IX.A.4 (Ground 1, claim 4), incorporated here, Hayasaki discloses this limitation.

Silverbrook also discloses this limitation. Ex. 1007 ¶ 271. Silverbrook explains that the "control logic 280 [red] is utilized to activate a heater element 281 [green]. Ex. 1005 at [0300], Fig. 76.

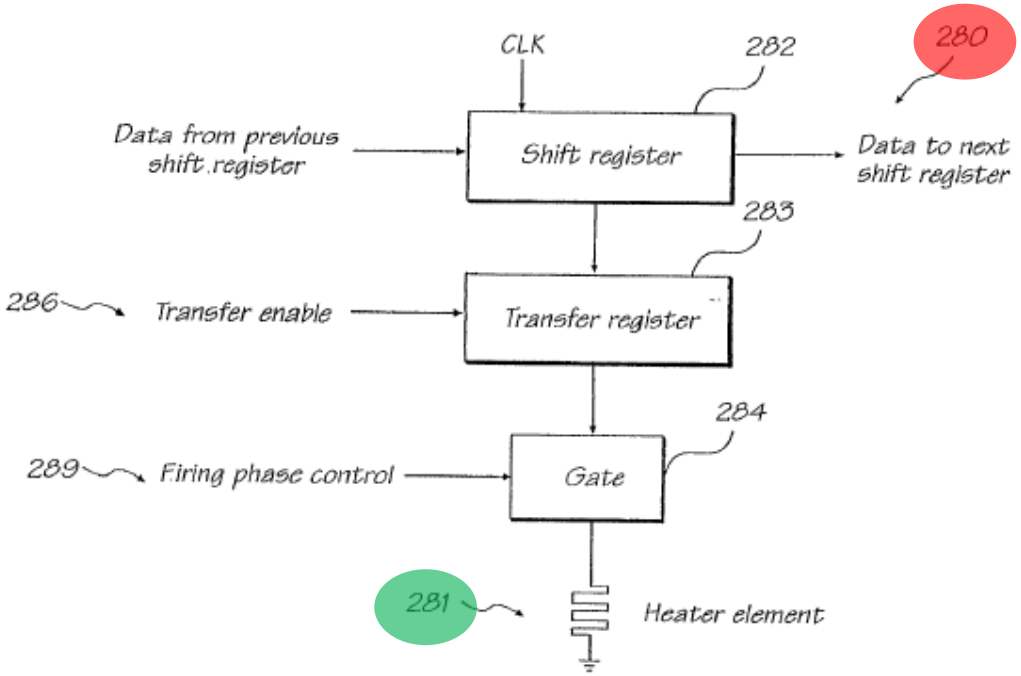


FIG. 76

Ex. 1004 at Fig. 76.

As seen in Figure 86 below, the first logic array (pink) addresses the first heater array (yellow), and the second logic array (blue) addresses the second heater array (red). Ex. 1005 at [0300, 0311-0312]; Fig. 86 below. The first logic array (pink) is **substantially parallel** to the second logic array (blue).

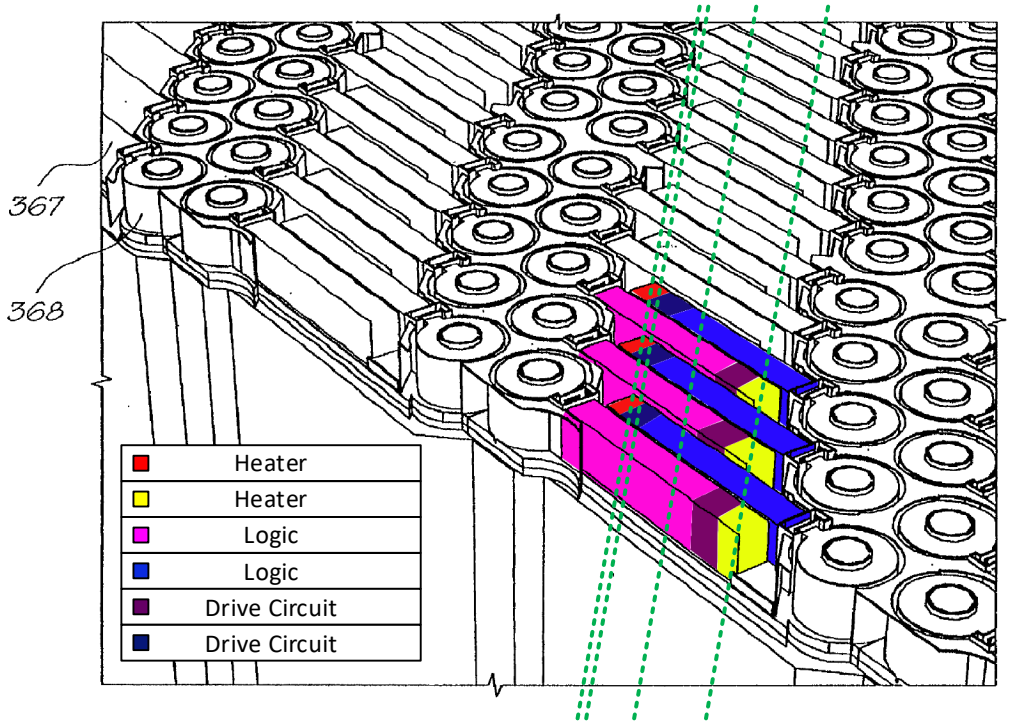


FIG. 86

4. Claim 5

Claim 5 requires "[t]he chip of claim 1, wherein the at least one logic array comprises a **single logic array** having **first logic cells for addressing the first heater array** and **second logic cells for addressing the second heater array**, wherein the single logic array is **substantially linear**." As discussed in Section IX.A.5 (Ground 1, claim 5), incorporated here, Hayasaki discloses this limitation.

Silverbrook also discloses this limitation because it too has a "single logic array" having first logic cells (pink) for addressing the first heater array (yellow) and second logic cells (blue) for addressing the second heater array (red). Ex. 1005 at

[0300, 0311-0312]; Fig. 86 below. The single logic array is substantially linear (here shown by the center green line). *See also* Section IX.B.1, incorporated here.

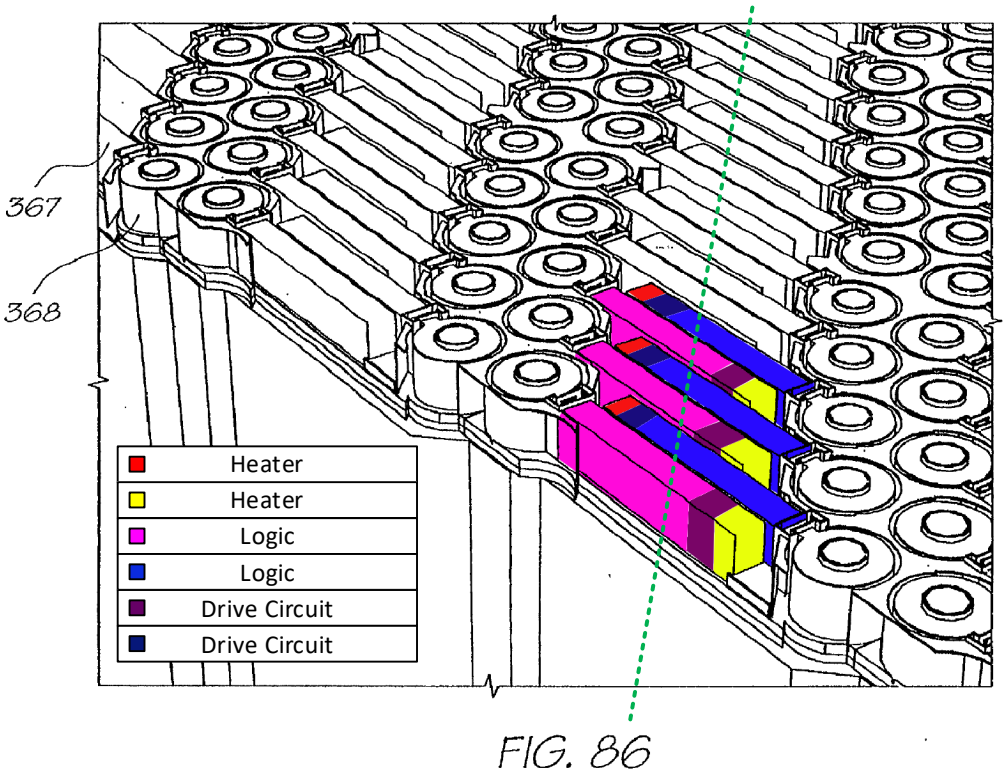


FIG. 86

Ex. 1005 at Fig. 86.

5. Claim 6

For the reasons discussed above in Section IX.B.1 (Ground 2, claim 1), incorporated here, Hayasaki as modified by Silverbrook discloses the limitations of claim 6.

6. Claim 7

Claim 7 requires "[t]he heater chip [of] claim 6, wherein **a pair of second logic cells** is **interleaved** between a **first pair of first logic cells** and a **second pair**

of first logic cells." As discussed in Section IX.A.7 (Ground 1, claim 7), incorporated here, Hayasaki discloses this limitation.

Silverbrook also discloses this limitation for similar reasons as described in Section IX.A.7. Because the plain language of the claim requires only that a "pair" of second logic cells be "interleaved" between a "first pair" of first logic cells and a "second pair" of first logic cells, Silverbrook discloses this. As in Figure 86 below, a "pair" of second logic cells (blue arrows) is interleaved between a first pair of first logic cells (pink arrows) and a second pair of first logic cells (green arrows).

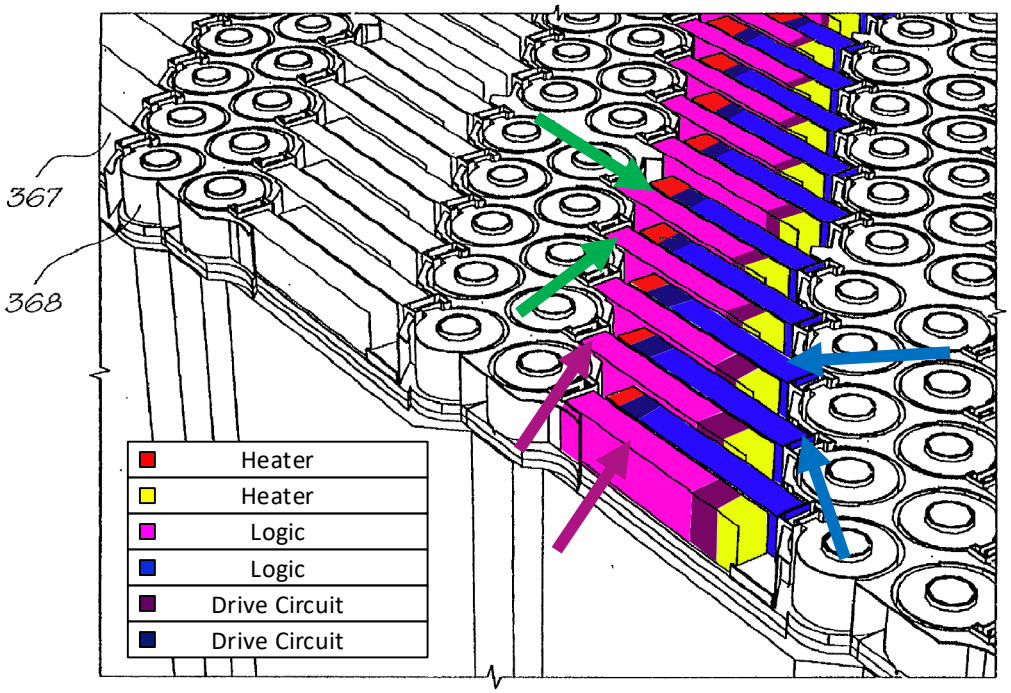


FIG. 86

7. Claim 8

For the reasons presented above for Ground 1, claim 8, Hayasaki discloses all of the elements of this claim. However, to the extent that the Board interprets this claim to require that all of the logic cells in need to be interleaved with one another, then the claim requirement that "the plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement is disclosed by Silverbrook for the reasons presented above with respect to the similar limitation in Ground 2, claim 1.

Therefore, Hayasaki in view of Silverbrook discloses **a first logic array** [e.g., Hayasaki's AND circuit arrays 5M' and its respective portion of wiring 8 and 5Y and its respective portion of wiring 8 or Silverbrook's purple and blue logic cells in Fig. 86 above] with the first logic array including a **plurality of first logic cells** [e.g., AND cells in Hayasaki 5M' + associated wiring in 8 or Silverbrook purple logic cells] and a **plurality of second logic cells** [e.g., AND cells in Hayasaki 5Y + associated wiring in 8 or Silverbrook blue logic cells] arranged in a **non-contiguous hybrid arrangement** [e.g., shift Hayasaki's first and second set of logic cells consistent with Figs. 85-86 of Silverbrook or replace Hayasaki's logic cells with Silverbrook's].

8. Claim 9

Claim 9 requires "[t]he heater chip of claim 8, wherein at least a portion of the first set of logic cells and at least a portion of the second set of logic cells are **substantially aligned**." As discussed in Section IX.A.9 (Ground 1, claim 9), incorporated here, Hayasaki discloses this limitation.

As seen in Figure 86 below, Silverbrook also discloses a portion of the first set of logic cells (pink) and at least a portion of the second set of logic cells (blue) are substantially aligned. Ex. 1007 ¶ 295.

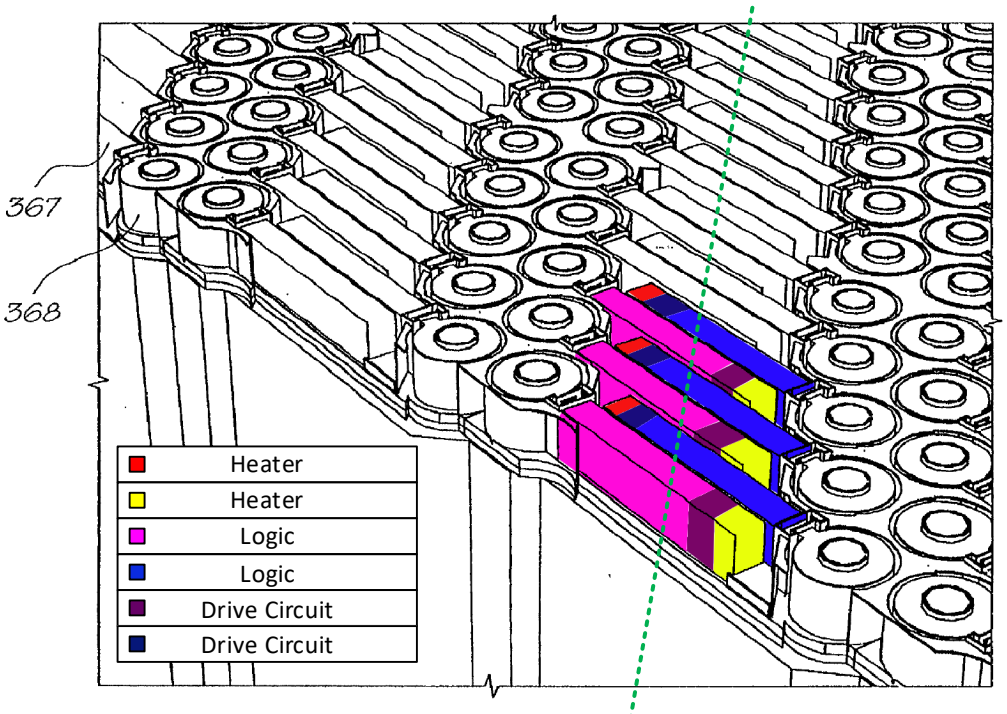


FIG. 86

9. Claim 10

Claim 10 requires that "the first logic cells are interleaved with the second logic cells." For the reasons discussed above in Section IX.B.8 (i.e., Ground 2, claim 8), incorporated here, Hayasaki as modified by Silverbrook discloses this limitation.

10. Claims 13-14

For the reasons discussed above in Section IX.A.13-14 (Ground 1, claims 13-14), incorporated here, Hayasaki discloses these limitations.

In light of the above, and for the reasons stated in the Section IX.B.1.a, a POSITA would have found claims 1-10 and 13-14 obvious over Hayasaki in view of Silverbrook.

C. Ground #3: Claims 1-10 and 13-14 are rendered obvious by Hayasaki and Krouss

1. Independent Claims 1 and 8

For the reasons presented above for Ground 1, claims 1 and 8, Hayasaki discloses all of the elements of these claims. To the extent the Board determines that Hayasaki does not disclose the claimed "first and second set of logic cells arranged in a **non-contiguous hybrid arrangement**," of claim 1 and the "plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement" of claim 8, then this element is clearly described in Krouss. Ex. 1007 ¶¶ ¶¶ 305-318.

Krouss describes a printhead 24 including "drop generators 30, 32, and 34 for depositing yellow, magenta, and cyan inks, respectively, on print media. Ex. 1012 at 6:54-57; Fig. 5.

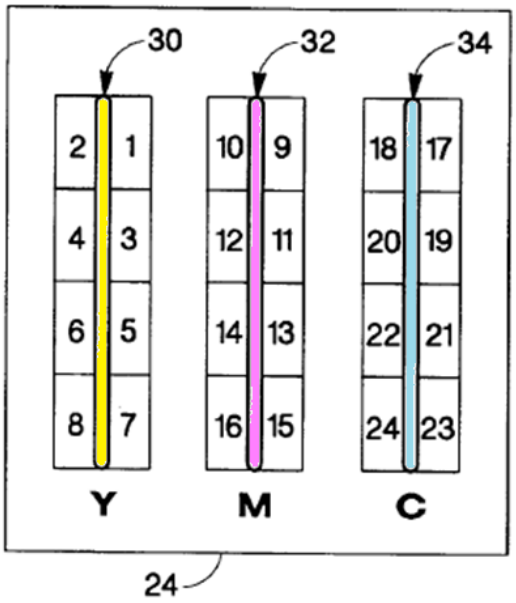


Fig. 5

Ex. 1012 at Fig. 5.

Figure 6 of Krouss (below) shows "the plurality of **drop generators 30** [yellow below] associated with yellow ink on printhead 24," and 48 represents an ink feed slot. Ex. 1012 at 6:65-7:5.

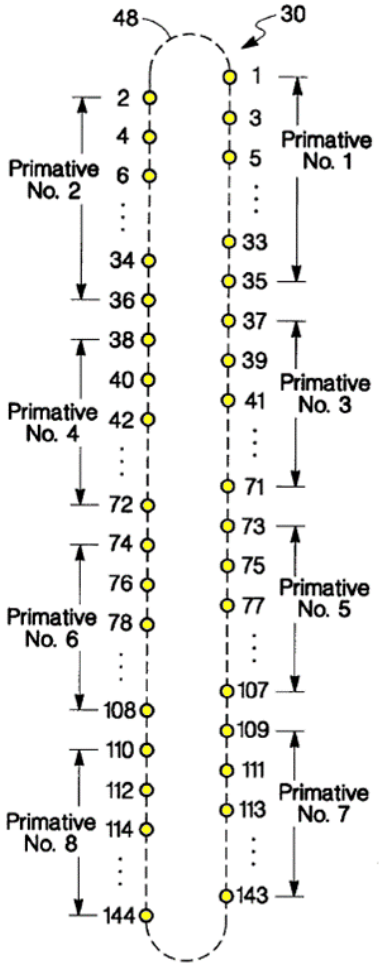


Fig. 6

Ex. 1012 at Fig. 6.

Krouss notes:

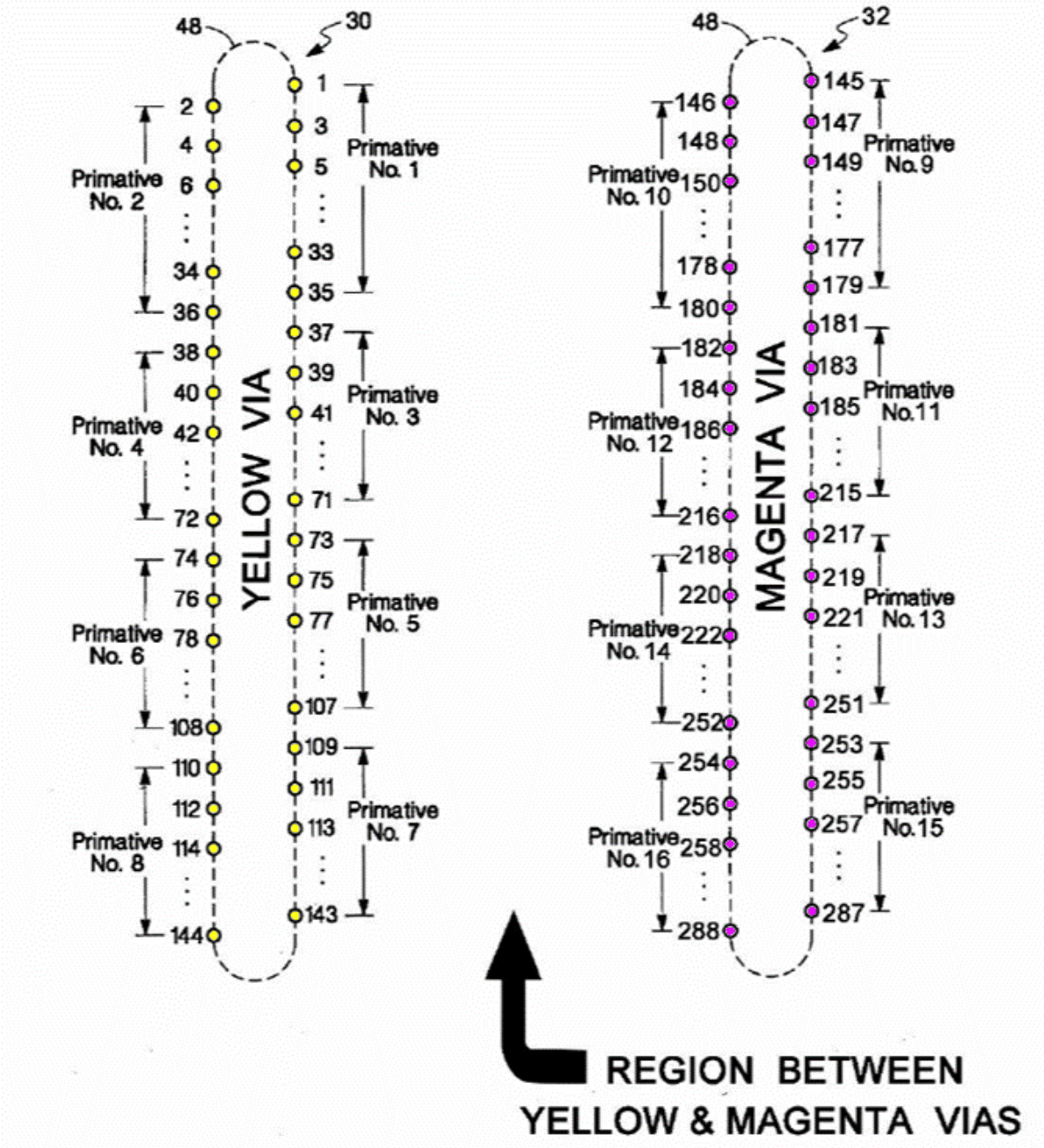
In the preferred embodiment, the **drop generators** are **arranged** in parallel rows adjacent the ink feed slot 48. The 144 **nozzles** associated with yellow ink drop (generators [sic] are each **offset** along a longitudinal axis of the ink feed slot 48. Each nozzle is numbered from 1 to 144 based on position along the longitudinal axis of the ink feed

> slot 48 with odd numbered nozzles on one side of the ink feed slot 48 and even numbered nozzles on the other side of the ink feed slot 48.

Ex. 1012 at 7:18-26.

Krouss also explains that "[t]he **drop generator layout** for the magenta ink feed slot 32 is **similar to the nozzle layout** for the yellow ink feed slot 30, except the nozzles are numbered from 145 to 288. Similarly, the drop generator layout for the cyan ink feed slot 34 is similar to the drop generator layout for the yellow ink feed slot 30 except the drop generator numbers range from 289 through 432." Ex. 1012 at 7:48-57.

Because of this drop generator offset arrangement, a POSITA would have understood that the magenta ink via's drop generator layout would also be offset as Dr. Curley has depicted below with the drop generators associated with the magenta ink via vertically offset as they are with the yellow ink via depicted in Figure 6:



Ex. 1007 ¶¶ 310-311. Thus, as shown above, the drop generators located on the right side of yellow ink via 48 are vertically interleaved with the drop generators located on the left side of magenta ink via 48. Ex. 1007 ¶ 312.

Table 1 of Krouss provides further information in that it discloses "address and primitive connections for each drop generator associated with the printhead 24." Ex. 1012 at 7:46-48.[6] "The drop generator number refers to the drop generator location along each of the ink feed slots 30, 32, and 34 for the yellow, magenta, and cyan inks, respectively." Ex. 1012 at 48-51.

A POSITA would have understood that Table 1 of Krouss teaches how to layout the drop generator positions and corresponding logic cell interconnects in the region between the yellow and magenta ink feed slots, including the specifics of the shared signal bus. A POSITA would have understood how to combine this information with Figures 5-6 to layout the geometry of the drop generators (and the corresponding logic cells) of the printhead. Ex. 1007 ¶¶ 313-318.

For example, Table 1 shows drop generator 1 (red box) corresponds with primitive 1 (blue box) and address 1 (purple box) while drop generator 3 (orange box) corresponds with primitive 1 (blue box) and address 12 (purple box). Ex. 1007 ¶ 314.

[6] As Krouss explains, "each resistor or drop generator is grouped into groups referred to as **primitives**." Ex. 1012 at 6:5-7.

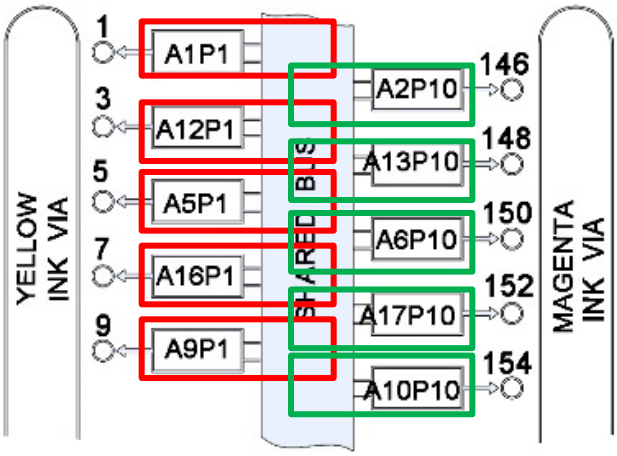
TABLE 1

ADDRESS AND PRIMITIVE FOR EACH DROP GENERATOR

	Yellow							
Primitive →	1	2	3	4	5	6	7	8
Address ↓								
1	1	28	37	64	91	82	127	118
2	11	2	47	38	101	92	137	128
3	21	12	57	48	75	102	111	138
4	31	22	67	58	85	76	121	112
5	5	32	41	68	95	86	131	122
6	15	6	51	42	105	96	141	132
7	25	16	61	52	79	106	115	142
8	35	26	71	62	89	80	125	116
9	9	36	45	72	99	90	135	126
10	19	10	55	46	73	100	109	136
11	29	20	65	56	83	74	119	110
12	3	30	39	66	93	84	129	120
13	13	4	49	40	103	94	139	130
14	23	14	59	50	77	104	113	140
15	33	24	69	60	87	78	123	114
16	7	34	43	70	97	88	133	124
17	17	8	53	44	107	98	143	134
18	27	18	63	54	81	108	117	144

Ex. 1012 at Fig. 1.

When this information in Table 1 is combined with Figures 5-6, a POSITA would have understood that the drop generators exhibit pitch doubling as Dr. Curely has illustrated below with a representative set of the first ten drop generators. Ex. 1007 ¶¶ 314-318.



GEOMETRY OF FIRST 10 SCAN LINES PER TABLE 1 OF KROUSS '000 DISCLOSURE

Ex. 1007 ¶¶ 316-317.

For the reasons presented below, a POSITA would have offset Hayasaki's heaters (e.g., as shown in Hayasaki's Fig. 9) and their associated circuitry (including their respective logic cells), as taught by Krouss. A POSITA would have understood that this would result in the first and second logic cells of Hayasaki arranged in a non-contiguous hybrid arrangement. Ex. 1007 ¶¶ 305-318.

a. Motivation to Combine Hayasaki and Krouss

A POSITA would have been motivated to modify Hayasaki's printhead by offsetting its heaters and associated logic cells (i.e., arranging the first and second sets of logic cells in a non-contiguous hybrid arrangement), as taught by Krouss.. Ex. 1007 ¶¶ 319-328.

First, Hayasaki and Krouss are **analogous** to the claimed subject matter in the '629 Patent as they all are within the **same field of endeavor** of multi-via printhead chips. Ex. 1004 at Abstract; Ex. 1005 at Abstract. The USPTO has also classified all three under the same classification number—U.S. Cl. 347. Ex. 1001 at 1; Ex. 1004 at 1; Ex. 1012 at 1.

Thus, Hayasaki and Krouss are analogous art that would have been considered by a POSITA. Ex. 1007 ¶ 322.

Second, a POSITA would have been motivated to combine Hayasaki and Krouss in order to make a smaller printhead that is reliable and inexpensive to manufacture with more dots-per-inch (and less expensive to make). A POSITA would have started with Hayasaki and then looked to improve reliability and reduce manufacturing costs by, for example, offsetting the heaters (and associated circuitry) as described in Krouss. Ex. 1007 ¶ 323.

A POSITA would have also been motivated to modify Hayasaki with Krouss in order to address the same problem identified by Hayasaki (cross-talk) while providing a good fault tolerance and high print quality. *See, e.g.*, Ex. 1004 at [0095]; Ex. 1012 at 7:65-8:12; Ex. 1007 ¶ 324.

Hayasaki explains that if "adjacent printing elements are to be driven concurrently, a phenomenon in which ink is insufficiently supplied adjacent nozzles (i.e., crosstalk) occurs because the inflow and outflow of ink occur at positions near

each other. In order to prevent the occurrence of this phenomenon, the circuits of the head substrate are configured so as not to drive adjacent printing elements concurrently, thus physically preventing the occurrence of this phenomenon." Ex. 1004 at [0095].

Krouss explains that "[b]ecause of the close proximity of drop generators within in each primitive, fluidic cross-talk between nearby drop generators can affect dynamic performance, such as ink chamber refill time. To avoid fluidic cross-talk problems, it is important that no more than one drop generator within each primitive be activated at the same time." Ex. 1012 at 8:5-12.

Krouss further explains that this problem of cross-talk is resolved by his address and primitive connections described in Table 1 because "each drop generator within each primitive has a unique address (Table 1) and because the address enable signals as shown in FIG. 7 are staggered in time and do not overlap then no more than one drop generator within each primitive will be activated at the same time." Ex. 1012 at 7:65-8:5.

Krouss's layout in Table 1 thus addresses the known problem of crosstalk identified by Hayasaki and also achieves a good "fault tolerance" while maintaining print quality. Ex. 1012 at 9:37-40, 9:63-10:4.

Given this, a POSITA would have been motivated to modify the printhead layout of Hayasaki to adopt the configuration described in Krouss's Table 1 in order

to eliminate cross-talk, as Hayasaki seeks to do, while maintaining print quality and limiting fault tolerance. Ex. 1007 ¶¶ 323-328.

2. Claims 2-5, 7, 9, and 13-14

For the reasons discussed above in Sections IX.A.2-5, IX.A.7, IX.A.9, IX.A.13-14 (Ground 1, Claims 2-5, 7, 9, 13-14), all incorporated here, Hayasaki discloses the limitations of these claims.

3. Claim 6

Claim 6 requires "[t]he chip of claim 5, wherein at least **a portion of the first logic cells are interleaved with at least a portion of the second logic cells**, thereby making the single logic array **non-contiguous**," which Hayasaki as modified by Krouss discloses as explained in Section IX.C.1 (Ground 3, claim 1), incorporated here.

4. Claim 10

Claim 10 requires "[t]he heater chip of claim 8, wherein the first logic cells are interleaved with the second logic cells, which Hayasaki as modified by Krouss discloses as described in Section IX.C.1 (Ground 3, claim 8), incorporated here.

In light of the above, and for the reasons stated in Section IX.C.1.a, a POSITA would have found claims 1-10 and 13-14 obvious over Hayasaki in view of Krouss.

X. SECONDARY CONSIDERATIONS

As it is the Patent Owner's burden to assert secondary considerations, to the extent that Patent Owner raises any such arguments in its Preliminary Response, Petitioners request authorization to respond thereto before any Institution Decision.

XI. CONCLUSION

Trial should be instituted, and the Challenged Claims should be cancelled as unpatentable.

Dated: September 2, 2022

Respectfully Submitted,

/ Dion M. Bregman /
Dion M. Bregman (Reg. No. 45,645)

U.S. PATENT NO. 7,559,629 – Claim Listing

No.	Claim Elements
Claim 1[P]	A chip for use in a printing device, comprising:
1[A]	a first heater array with a left side and a right side;
1[B]	a first ink via placed on the left side of the first heater array;
1[C]	a second heater array with a left side and a right side, wherein a right side of the first heater array faces the left side of the second heater array;
1[D]	a second ink via placed on the right side of the second heater array; and
1[E]	at least one logic array including a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement, the at least one logic array is disposed substantially between the first heater array and the second heater array, wherein the first set of logic cells addresses and controls the first heater array and the second set of logic cells addresses and controls the second heater array, which allows the first ink via and second ink via to be simultaneously controlled by the at least one logic array, and
1[F]	wherein the at least on logic array is substantially parallel with the first heater array and second heater array.
Claim 2	The chip of claim 1, further comprising a third heater array and a fourth heater array, wherein the third heater array and first heater array sandwich the first ink via and the fourth heater array and the second heater array sandwich the second ink via.
Claim 3	The chip of claim 1, wherein the first and second ink via comprise one of a cyan ink via, a magenta ink via, a yellow ink via, and monochrome ink via.
Claim 4	The chip of claim 1, wherein the at least one logic array includes a first logic array for addressing the first heater array and a second logic array for addressing the second heater array, wherein the first logic array is substantially parallel to the second logic array.
Claim 5	The chip of claim 1, wherein the at least one logic array comprises a single logic array having first logic cells for addressing the first heater array and second logic cells for addressing the second heater array, wherein the single logic array is substantially linear.
Claim 6	The chip of claim 5, wherein at least a portion of the first logic cells are interleaved with at least a portion of the second logic cells, thereby making the single logic array non-contiguous.

Claim 7	The heater chip claim 6, wherein a pair of second logic cells is interleaved between a first pair of first logic cells and a second pair of first logic cells.
Claim 8[P]	An integrated multi-via heater chip, comprising;
8[A]	a first heater array having a left side and a right side;
8[B]	a first ink via positioned on the left side of the first heater array;
8[C]	a second heater array having a left side and a right side, wherein the first heater array and the second heater array are positioned opposite one another so that the right side of the first heater array is facing the left side of the second heater array;
8[D]	a second ink via positioned on the right side of the second heater array;, and
8[E]	a first logic array positioned substantially between the first heater array and the second heater array, wherein the first logic array includes a plurality of first logic cells for addressing and controlling the first heater array and a plurality of second logic cells for addressing and controlling the second heater array, the plurality of first logic cells and the plurality of second logic cells are arranged in a non-contiguous hybrid arrangement which allows the first ink via and second ink via to be simultaneously controlled by the first logic array, and
8[F]	wherein the first logic array is substantially parallel with the first heater array and second heater array.
Claim 9	The heater chip of claim 8, wherein at least a portion of the first set of logic cells and at least a portion of the second set of logic cells are substantially aligned.
Claim 10	The heater clip of claim 8, wherein the first logic cells are interleaved with the second logic cells.
Claim 13	The heater chip claim 8, wherein at least a portion of control signals for the first logic cells are routed between the first heater array and the first logic array and wherein at least a portion of control signals for the second logic cells are routed between the second heater array and the first logic array.
Claim 14	The heater chip of claim 8, wherein the first heater array comprises a plurality of blocks of heaters and the second heater array comprises a plurality of blocks of heaters, wherein each block of heaters in the first heater array is addressed by at least a portion of the first logic cells and wherein each block of heaters in the second heater array is addressed by at least a portion of the second logic cells.

CERTIFICATION OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Petition includes 13,919 words as counted by Microsoft Word and is therefore in compliance with the 14,000 word limit established by 37 C.F.R. 42.24(a)(1)(i). Accordingly, pursuant to 37 C.F.R. 42.24(d), lead counsel for the Petitioner hereby certifies that this Petition complies with the type-volume limits established for a petition requesting IPR.

Dated: September 2, 2022

Respectfully Submitted,

/ Dion M. Bregman /
Dion M. Bregman (Reg. No. 45,645)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. 42.6(4) and 42.105, lead counsel for Petitioners hereby certifies that on September 2, 2022, copies of this Petition and all supporting exhibits were sent via Priority Mail Express to the correspondence address of record for the '629 patent:

133676 - Goldberg Segalla LLP
711 3rd Avenue, Suite 1900
New York, NY 10017

A courtesy copy of this Petition and supporting exhibits was also served via email on September 2, 2022 on Patent Owner's counsel of record in the district court litigation against Slingshot Printing LLC involving this patent:

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Dated: September 2, 2022

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